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49	1394 VIA 6308S
50	+VCORE Controller
51	+VCORE Phasel & Phase2
52	+VCORE Phase3 & Phase4
53	+5V_Dual & +5V_Dual_USB_B
54	+3P3VSB
55	+1P8V_Dual & +VTT_DDR
56	NB/SB 1P125V Power
57	+1P2V_FSB_VTT & +1P5V
58	Blank
59	Blank

# LENOVO G43

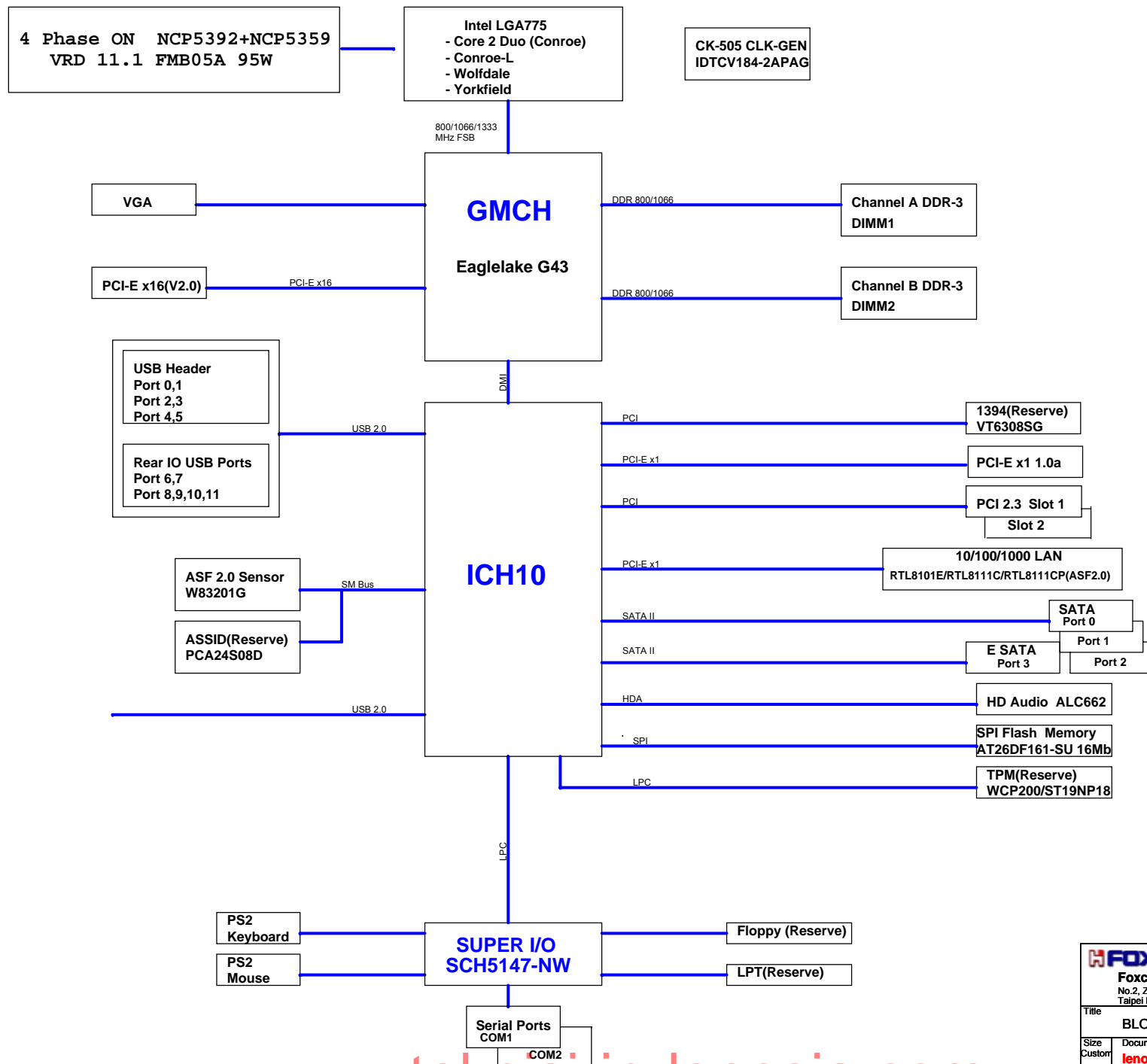
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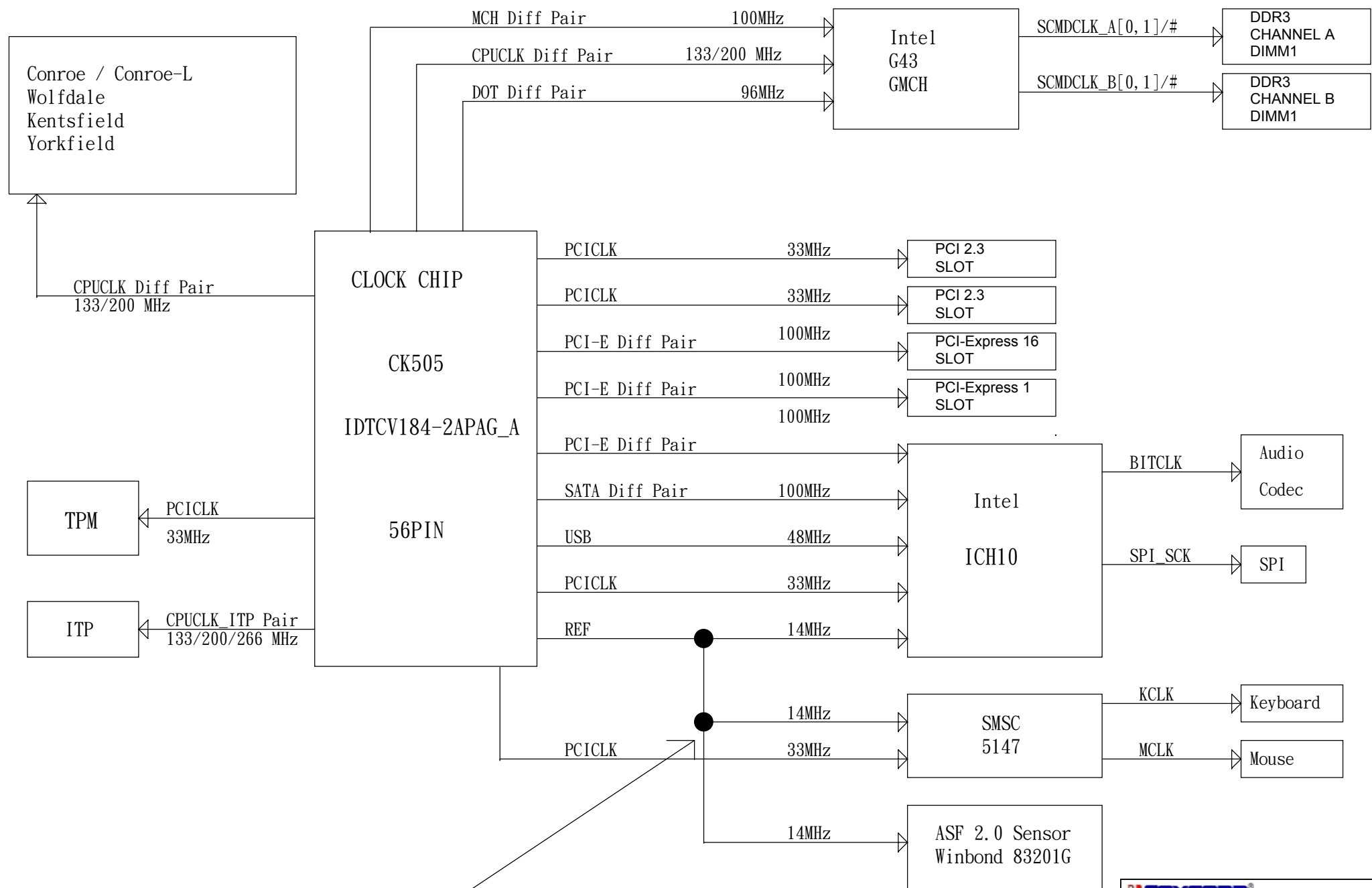
## Lenovo Requirement

- Material Need to follow Lenovo "Lenovo Control BOM.
- To avoid BGA crack that using GND pin for ICT

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Title TOC / SCH CHANGES			
Size Custom	Document Number Lenovo G43	Rev X1	
Page Modified Tuesday, March 04, 2008		004629 (UTC/GMT)	Sheet 1 of 59


# BLOCK DIAGRAM

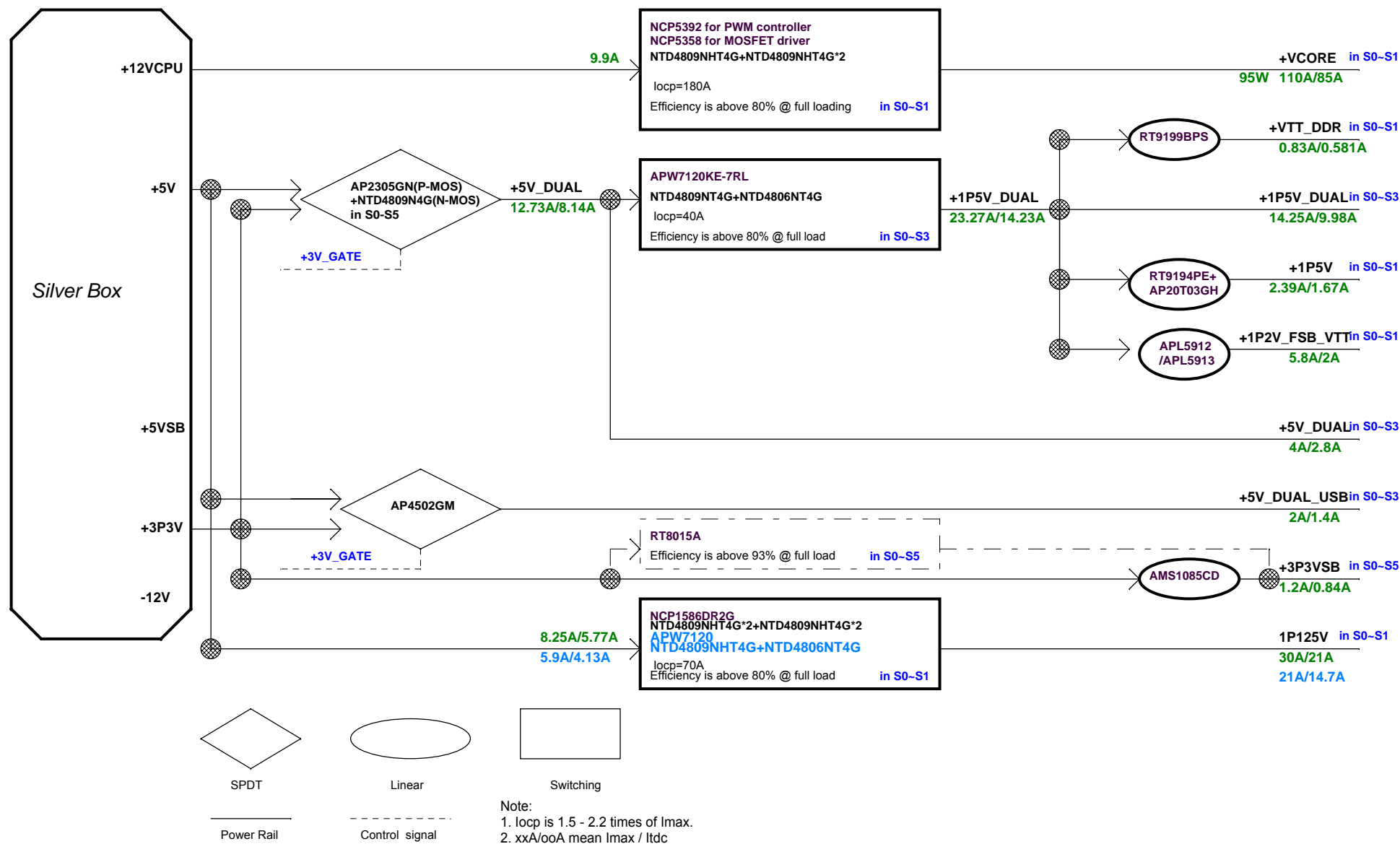


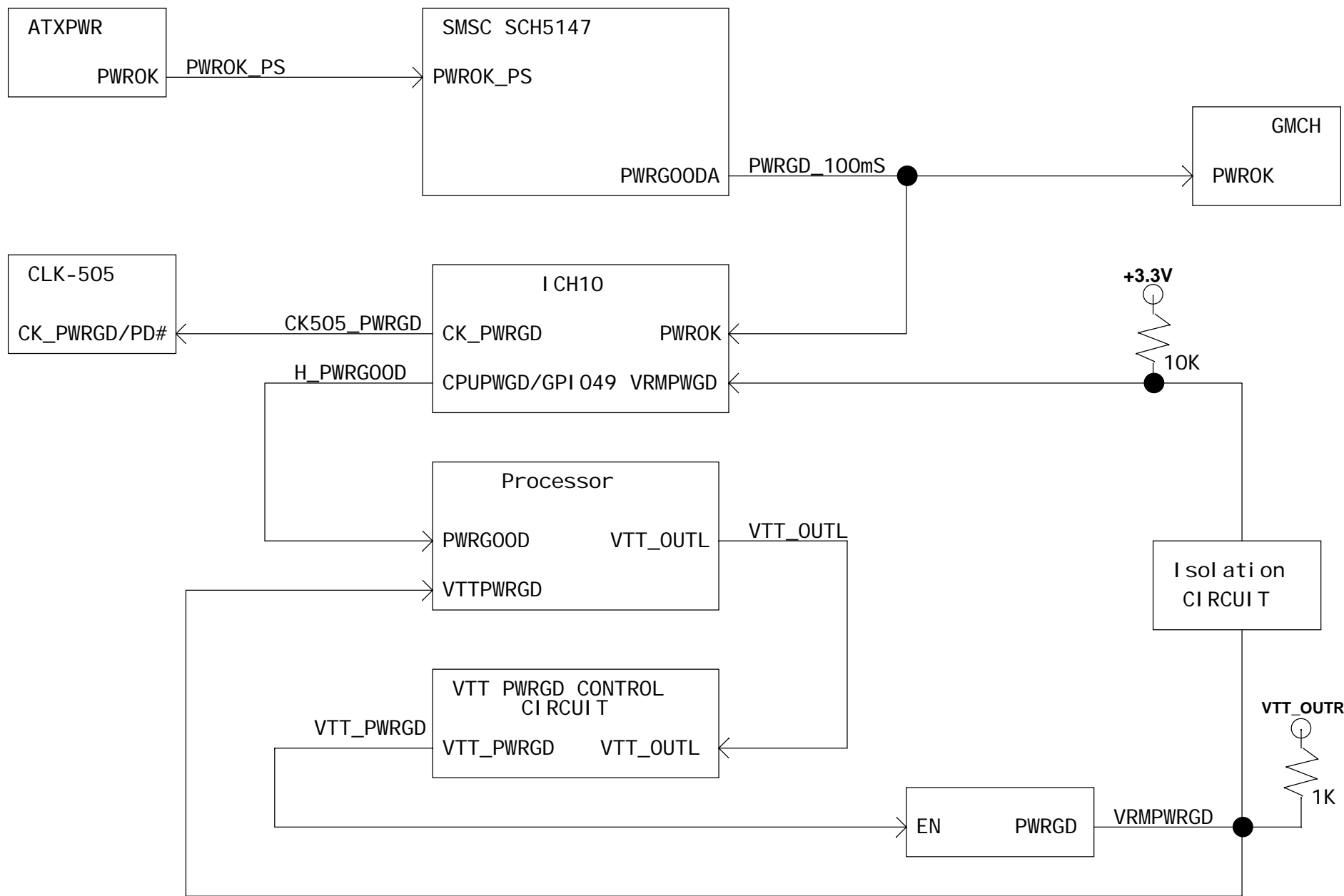


One Source Driver 3 device  
High Risk

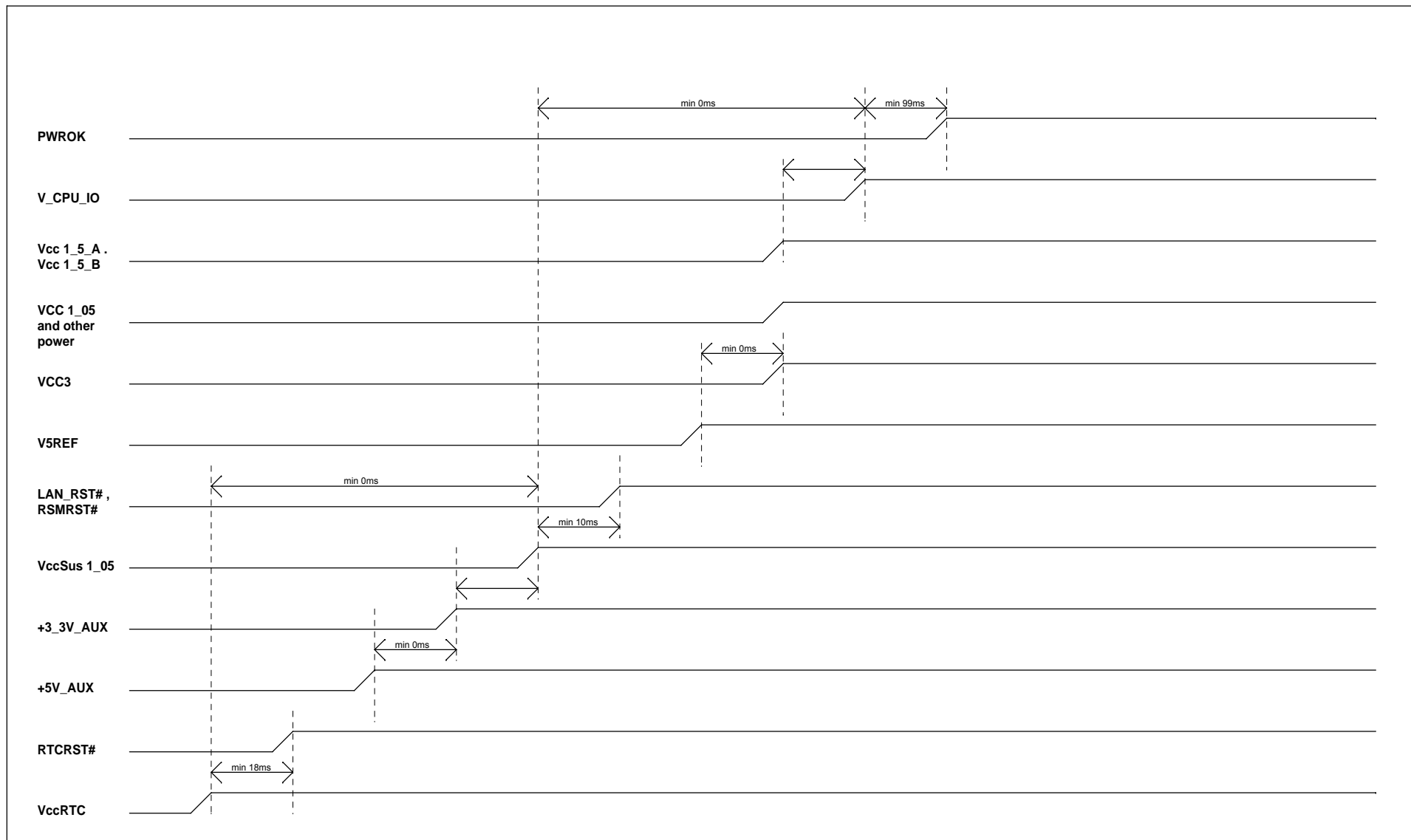


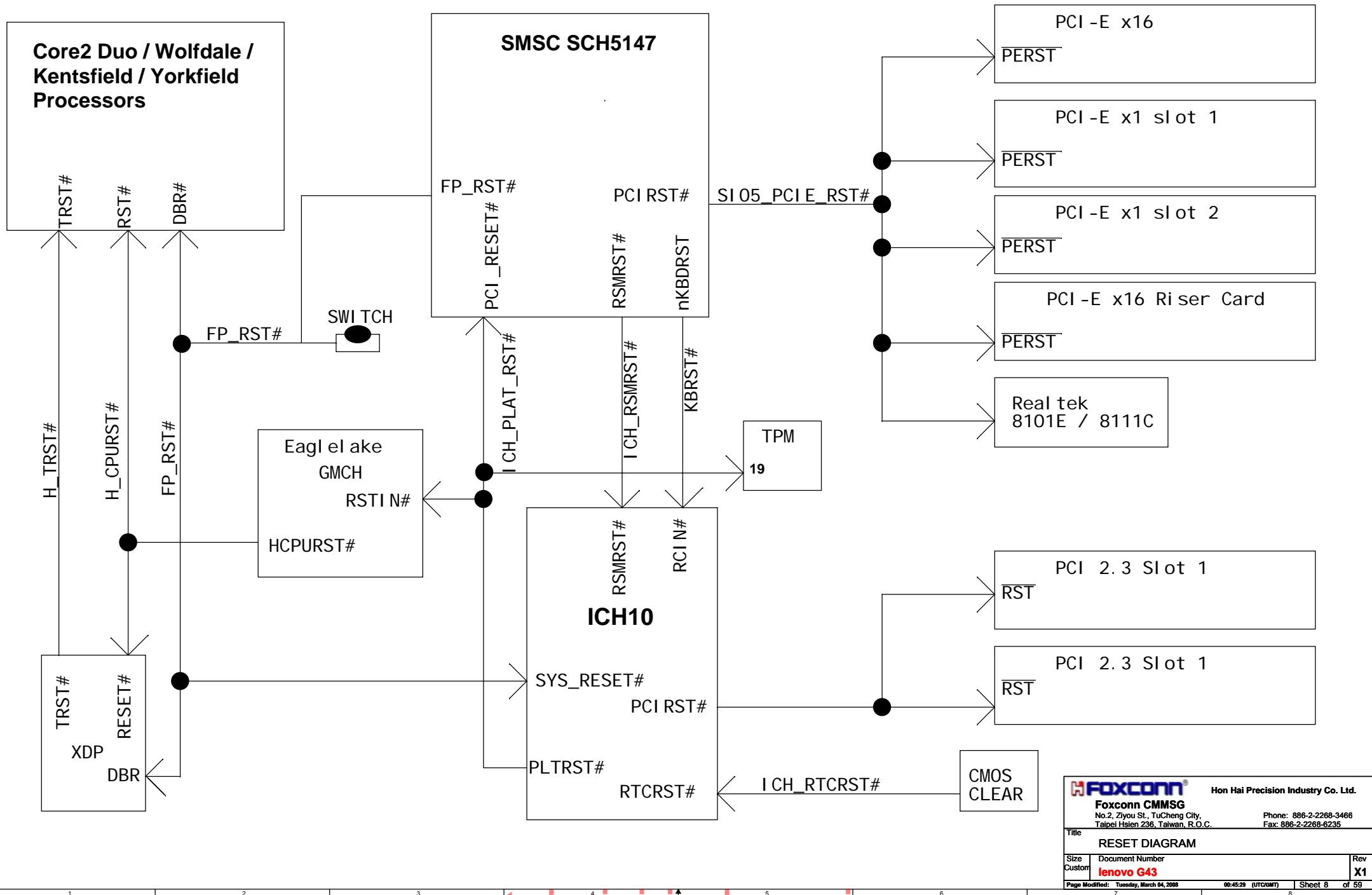
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Title			
<b>POWER DISTRIBUTION DIAGRAM</b>			
Size Custom	Document Number <b>lenovo G43</b>		Rev <b>X1</b>
Page Modified: Tuesday, March 04, 2008		08:45:30 (UTC+8MT)	Sheet 4 of 59



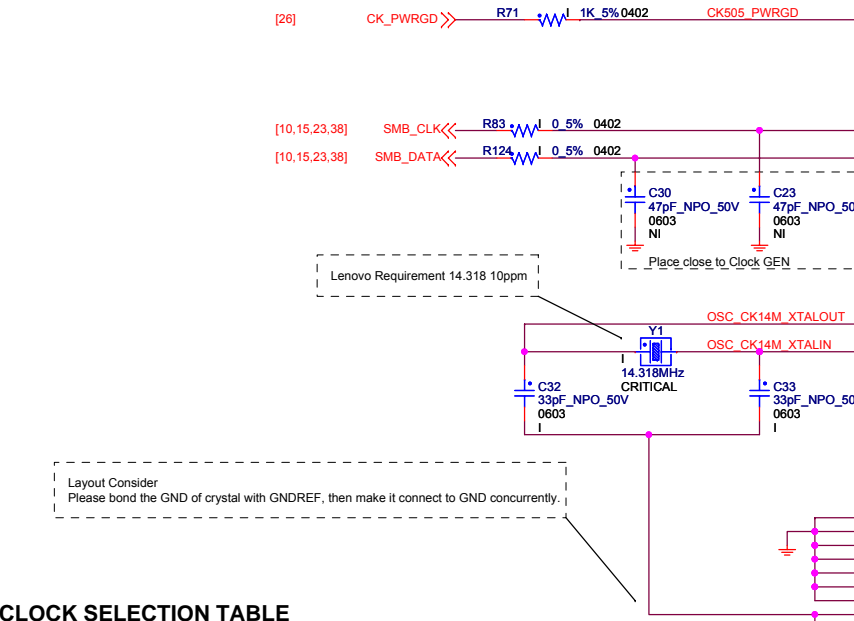


# POWER SEQUENCE DIAGRAM

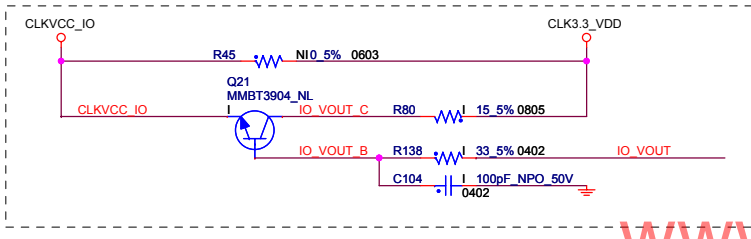




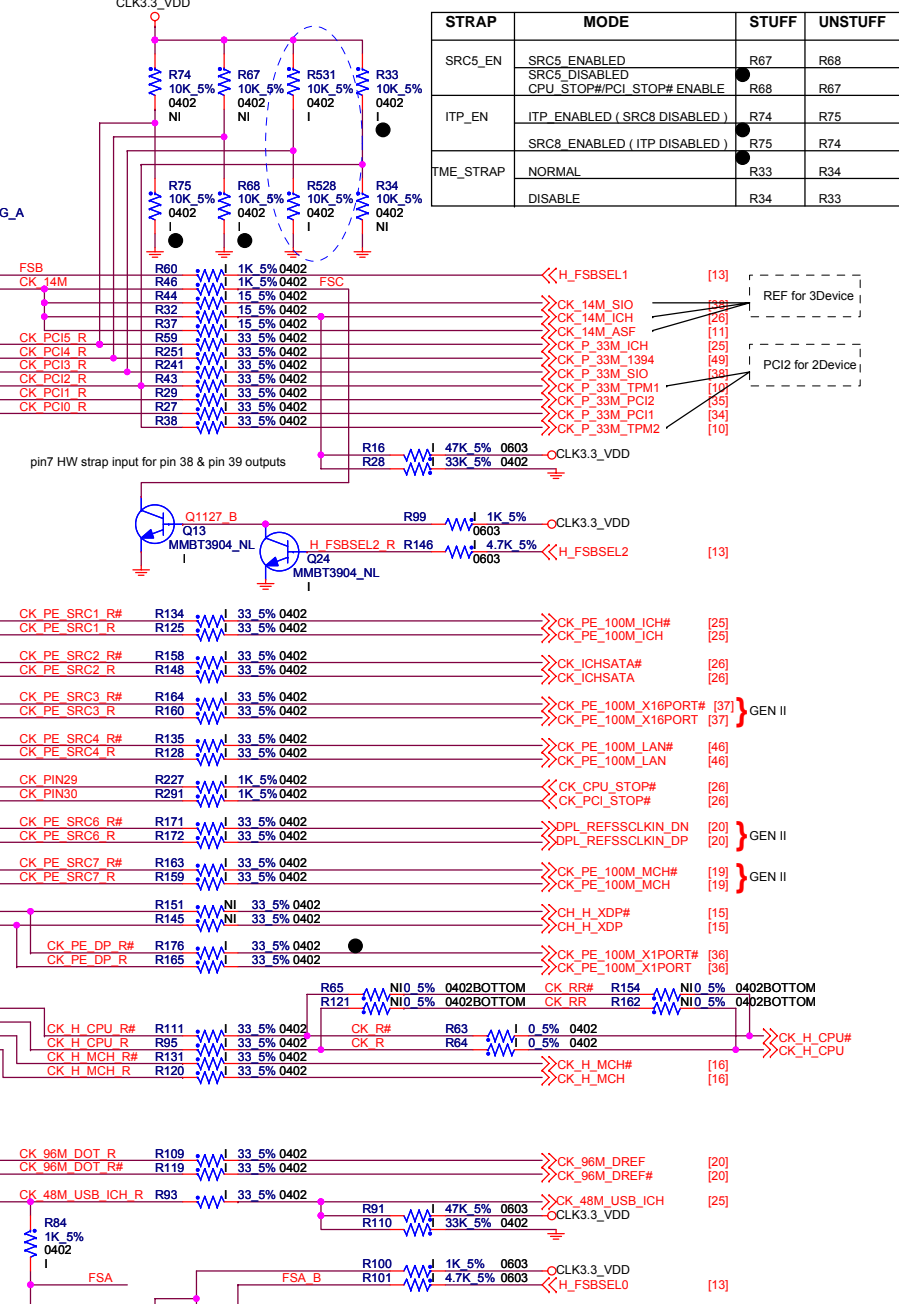
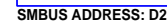





FSC	FSB	FSA	CPU
0	1	0	200
0	0	0	266
1	0	0	333

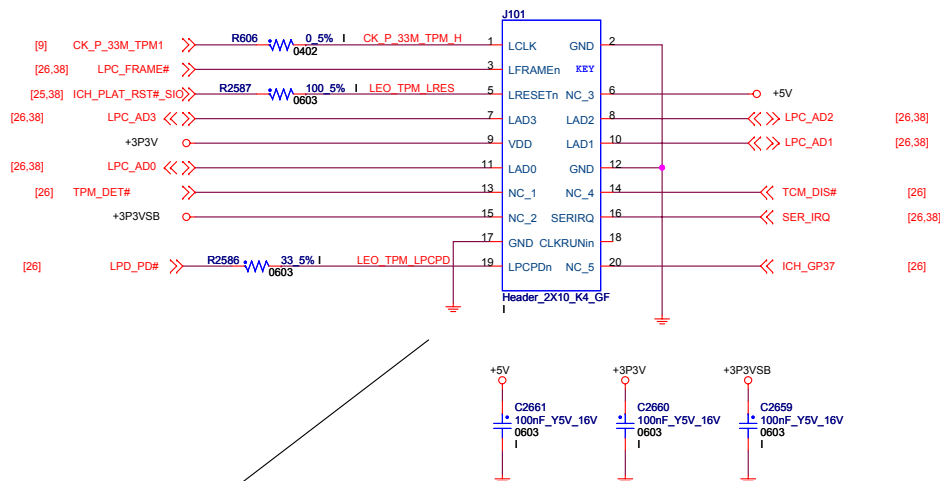
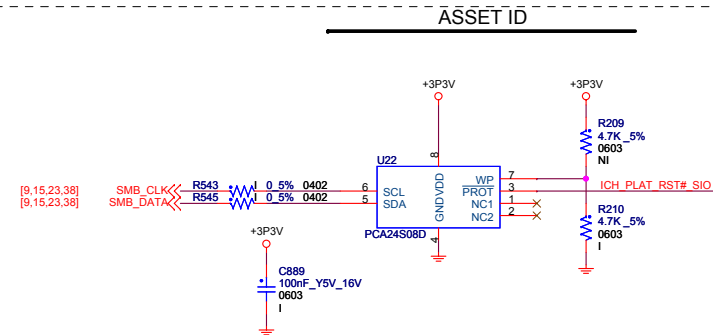


Pin12 : ( 0.1uF )  
Pin20 : ( 0.1uF ), ( 10uF )  
Pin26 : ( 0.1uF ), ( 10uF )  
Pin31 : ( 0.1uF )  
Pin37 : ( 0.1uF ), ( 10uF )  
Pin41 : ( 0.1uF ), ( 10uF )  
Pin47 : ( 0.1uF )  
Pin53 : ( 4.7uF ), ( 0.1uF )

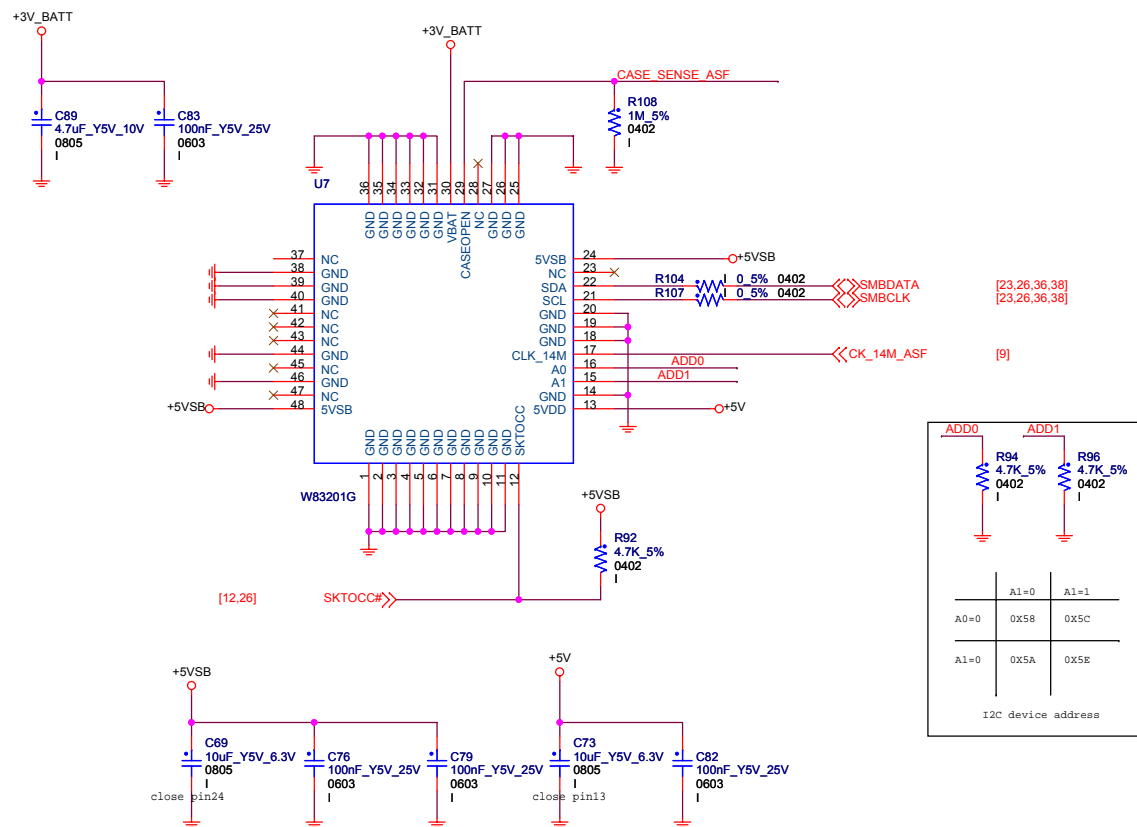


STRAP	MODE	STUFF	UNSTUFF
SRC5_EN	SRC5_ENABLED	R67	R68
	SRC5_DISABLED CPU_STOP#PCI_STOP#ENABLE	R68	R67
ITP_EN	ITP_ENABLED (SRC8_DISABLED)	R74	R75
	SRC8_ENABLED (ITP_DISABLED)	R75	R74
TME_STRAP	NORMAL	R33	R34
	DISABLE	R34	R33

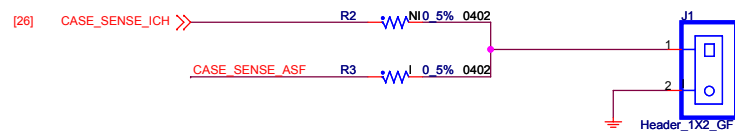
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<b>Title</b>			
<b>CLOCK GEN - CK505</b>			
<b>Size Custom</b>	<b>Document Number</b>  <b>lenovo G43</b>		<b>Rev</b>  <b>X1</b>
<b>Page Modified: Tuesday, March 04, 2008</b>		<b>00:45:30 (UTC+GMT)</b>	<b>Sheet 9 of 59</b>



```
LEO_CHIP Header Pin Define:
13pin : Detect card
- L : have card
- H: no card
14pin: Disable/enable TCM function
20pin: No function now, only tied to SB GPIO
```



**Lenovo Case Open**  
**Special Material need to check AND make sure Pin1.**

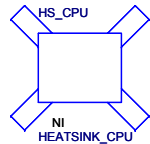
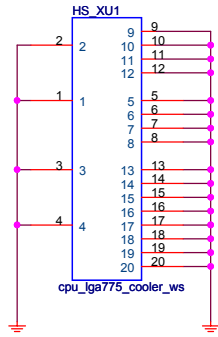


# P4 LGA775 Signals 1

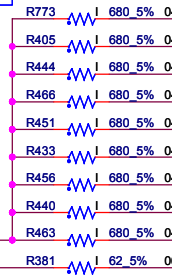
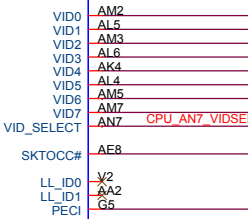
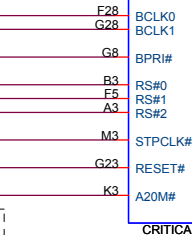
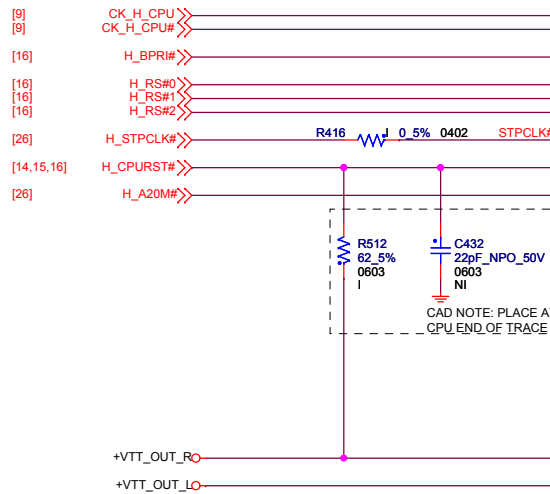
XU1A LGA775\_15u

H\_A#[3..35]

CAD NOTE: ADDRESS: SIGNAL(S) ROUTE WITHIN SAME GROUP TO +/-25 MILS AND MUST BE LENGTH MATCHED TO THE STROBE.



NI HEATSINK\_CPU



CAD NOTE: PLACE AT CPU END OF TRACE

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Title

**P4 LGA775 Signals 1**

Size

Custom

Document Number

**lenovo G43**

Rev

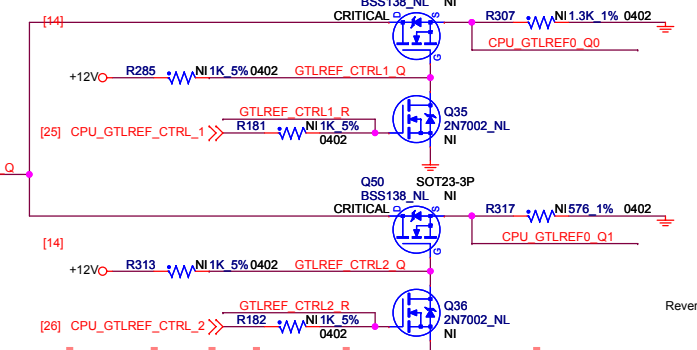
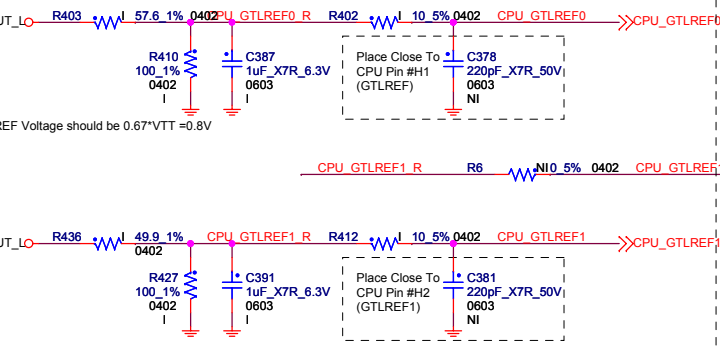
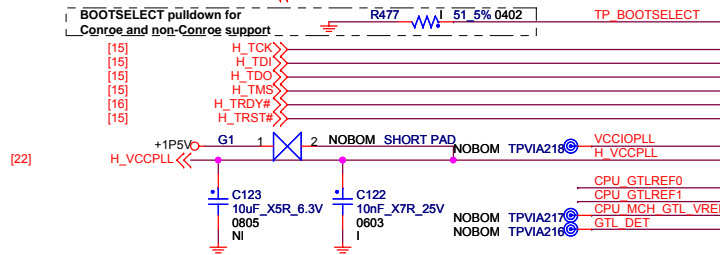
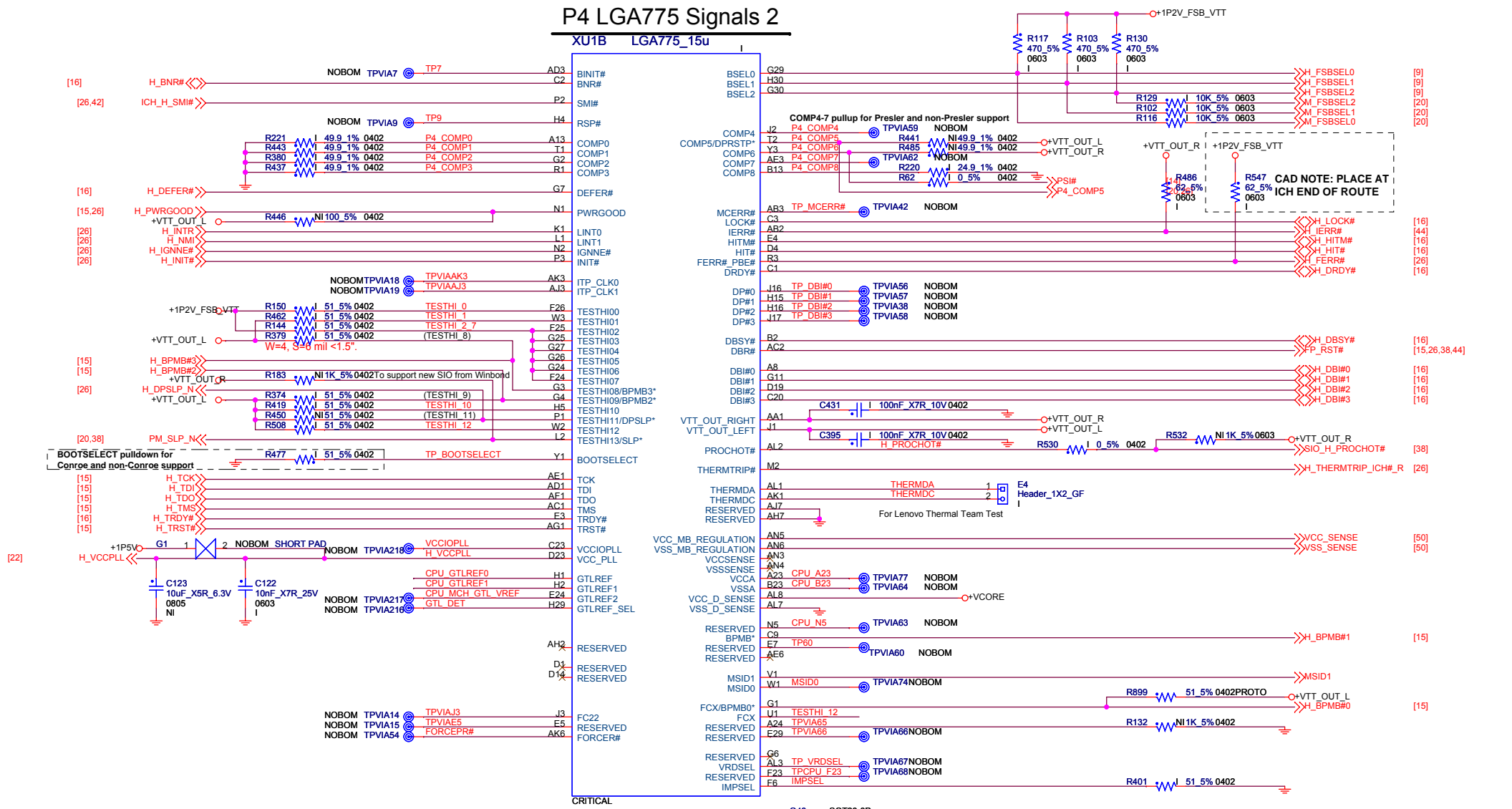
**X1**

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# P4 LGA775 Signals 2

XU1B LGA775\_15u



STATE	CONROE SUPPORT	NON-CONROE SUPPORT
BOOTSELECT	R477 (I)	R477 (NI)
MSID	R454_0 ohm(I), R162 (I), R15 (NI)	R454_51 ohm(I), R162 (NI), R15 (I)
COMP4-7	R408, R441, R485, R488 all (NI)	R408, R441, R485, R488 all (I)
VID SELECT	R575 (NI) VRD11-- on page:12	R575 (I) VR10/VR11 -- on page:12

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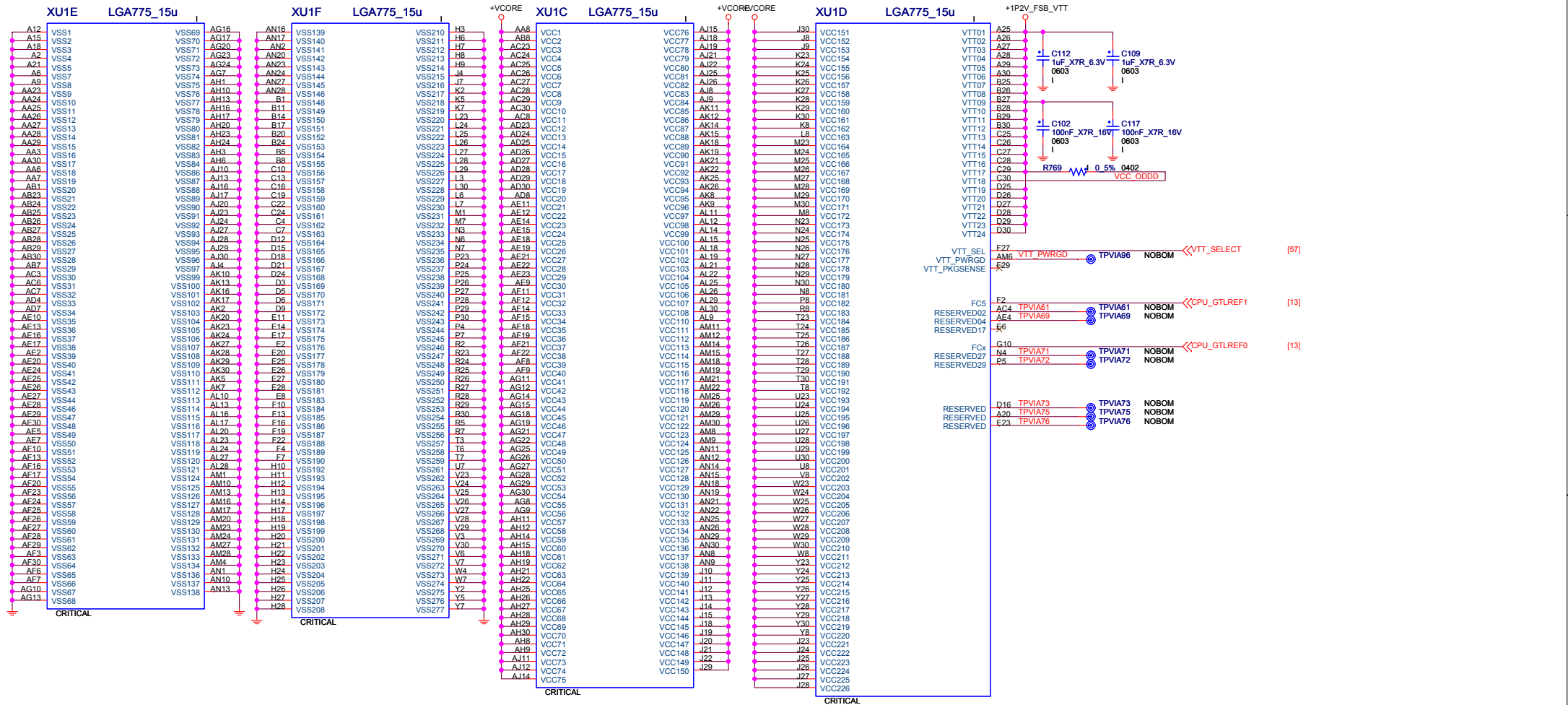
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Fax: 886-2-2268-6235

Title: **P4 LGA775 Signals 2**

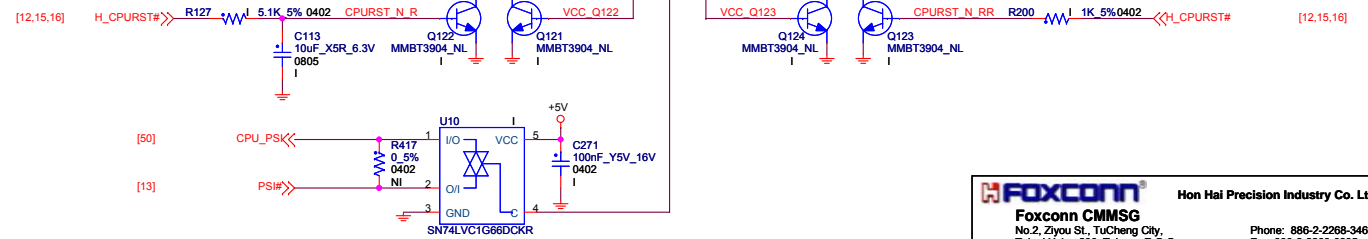
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# P4 LGA775 Power

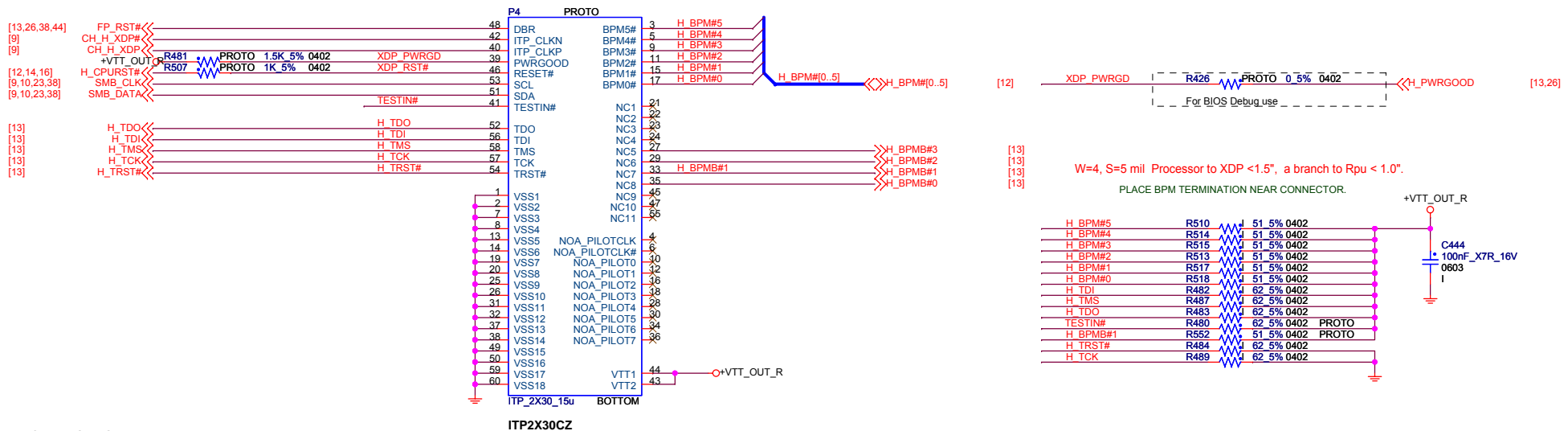


C-step Erratum for PSI  
 Wolflake and Yorkfield processors have a C-step erratum for PSI  
 - The PSI# signal will improperly be asserted during power-on  
 - The assertion will occur while the processor RESET# is asserted  
 - The assertion will extend beyond RESET# signal deassertion for a short duration  
 - After completing power-on, the PSI# signal will not assert for C-step  
 - E-step has a planned fix for this erratum  
 - Intel designed, and will validate, a circuit to work around this erratum  
 - The circuit blocks the errant PSI# signal assertion, only allowing the PSI# signal to pass to the VR after ~50ms after RESET# is deasserted (see later slide)  
 - Objective was to enable a circuit to allow for a single Eaglelake board BOM that is compatible with C-step (without PSI support) and E-step (with PSI support)





## Intel XDP Debugging Connector



### XTP CAD NOTES:

- Place XP port 2 to 4 inches from processor in solder side.
- Match Impedance of the BPM signals to 50 ohm and trace width to 5 mils with 10 mil spacing.
- TCK signal spacing should be 5 mil trace and 10 mil spacing. TCK should split at the XTP and route to CPU.
- FBO signal spacing should be 5 mil trace and 10 mil spacing. Match FBO length to the length of BPM segment from XTP to CPU.
- TMS# signal spacing should be 5 mil trace and 10 mil spacing. Route in daisy chain with pull-up at XTP port.
- TRST# signal spacing should be 5 mil trace and 10 mil spacing. Route in daisy chain starting from XTP to CPU.
- CPU\_RST# signal spacing should be 5 mil trace and 10 mil spacing. Route in daisy chain starting from GMCH to CPU.
- TDI, TDO signal spacing should be 5 mil trace and 10 mil spacing.
- Other signals should have 5 mil trace and 10 mil spacing.

### CPU XDP TERMINATION.

BPM#[0.5]: the length accounts for both the distance from the CPU to XDP connector and the sub to the termination should less than 1.5".

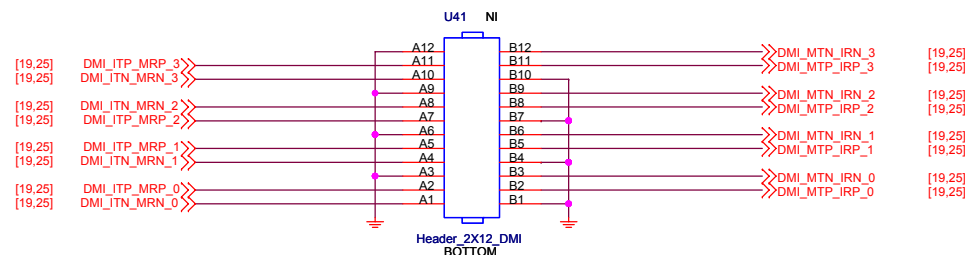
PLACE TMS/TDI TERMINATION NEAR CPU WITHIN 1.5" OF CPU.

PLACE TDO TERMINATION NEAR CONNECTOR.

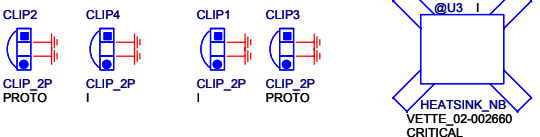
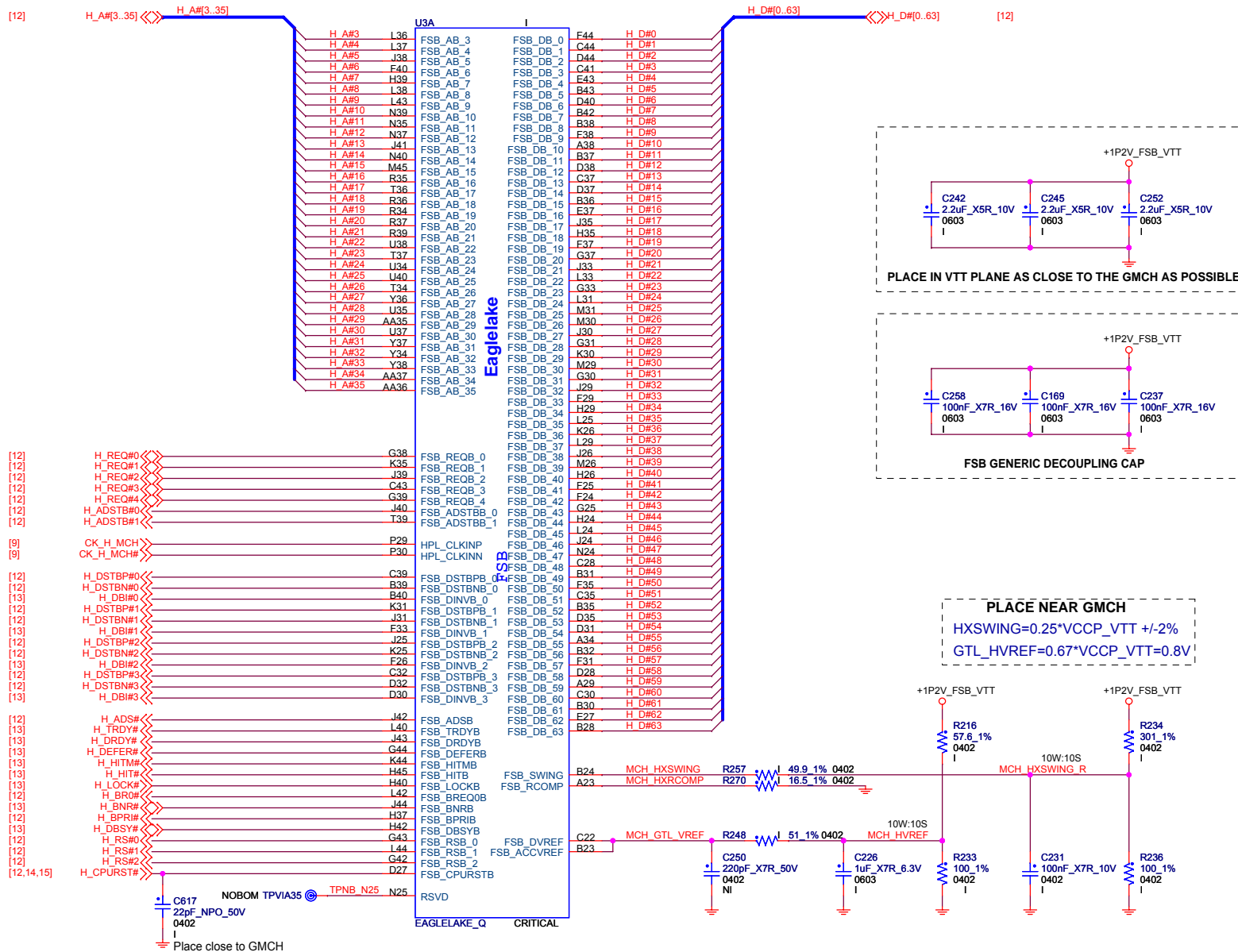
PLACE TCK TERMINATION NEAR CPU WITHIN 1.5" OF CPU.

PLACE TRST# TERMINATION ANYWHERE ON ROUTE.

## Intel DMI Debug Connector



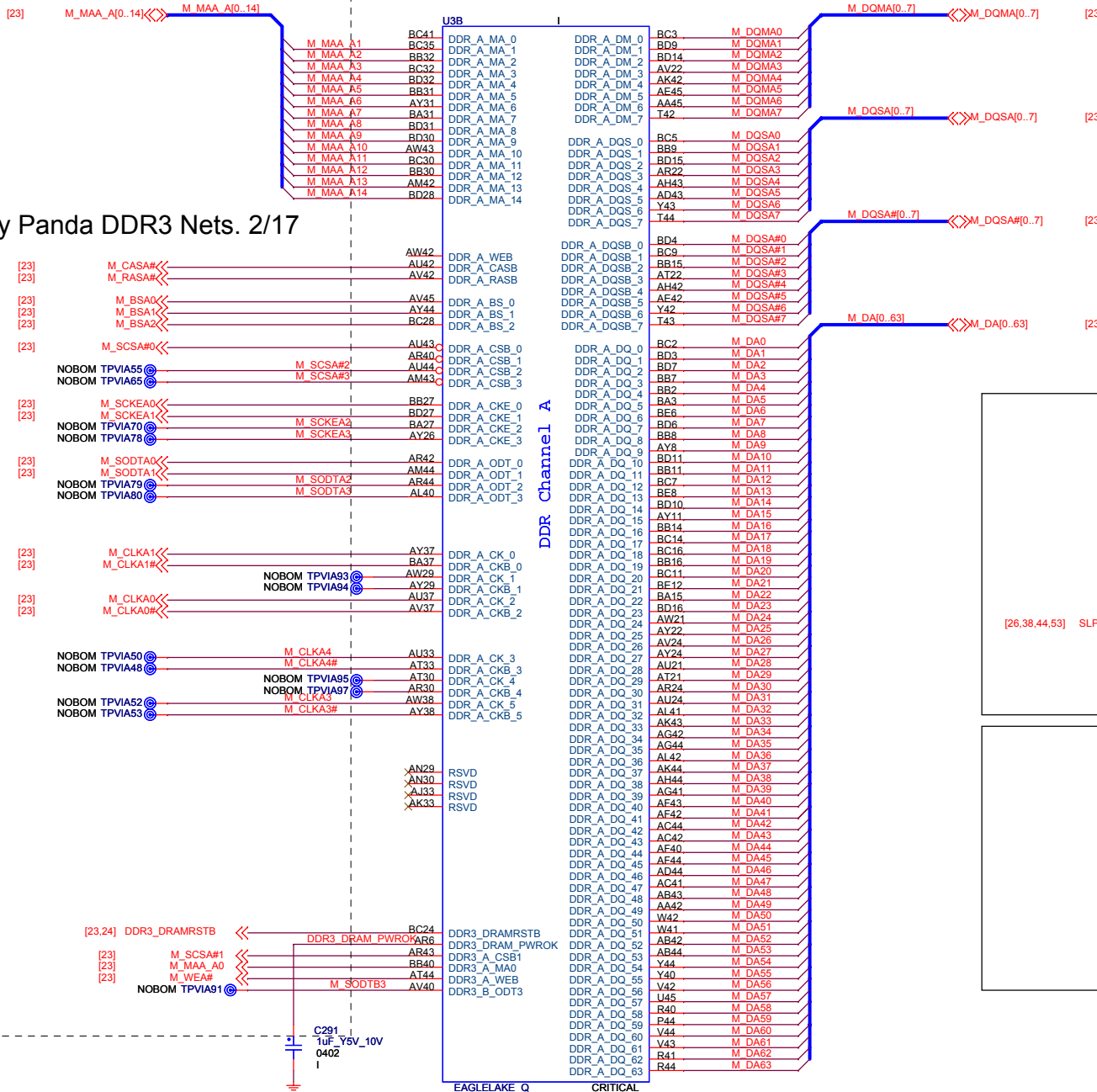
# MCH-CPU FSB Interface



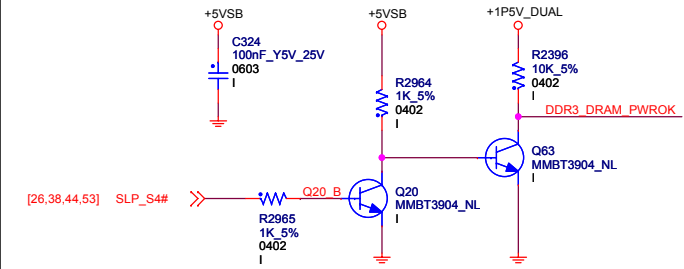


# MCH-DDR3 Memory Channel A

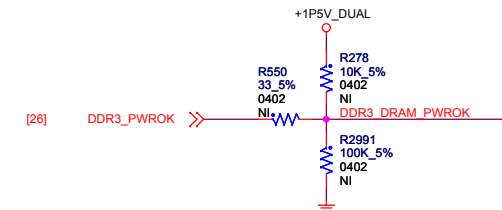
Copy Panda DDR3 Nets. 2/17



## DRAM PWROK Option when usign ICH10 Base

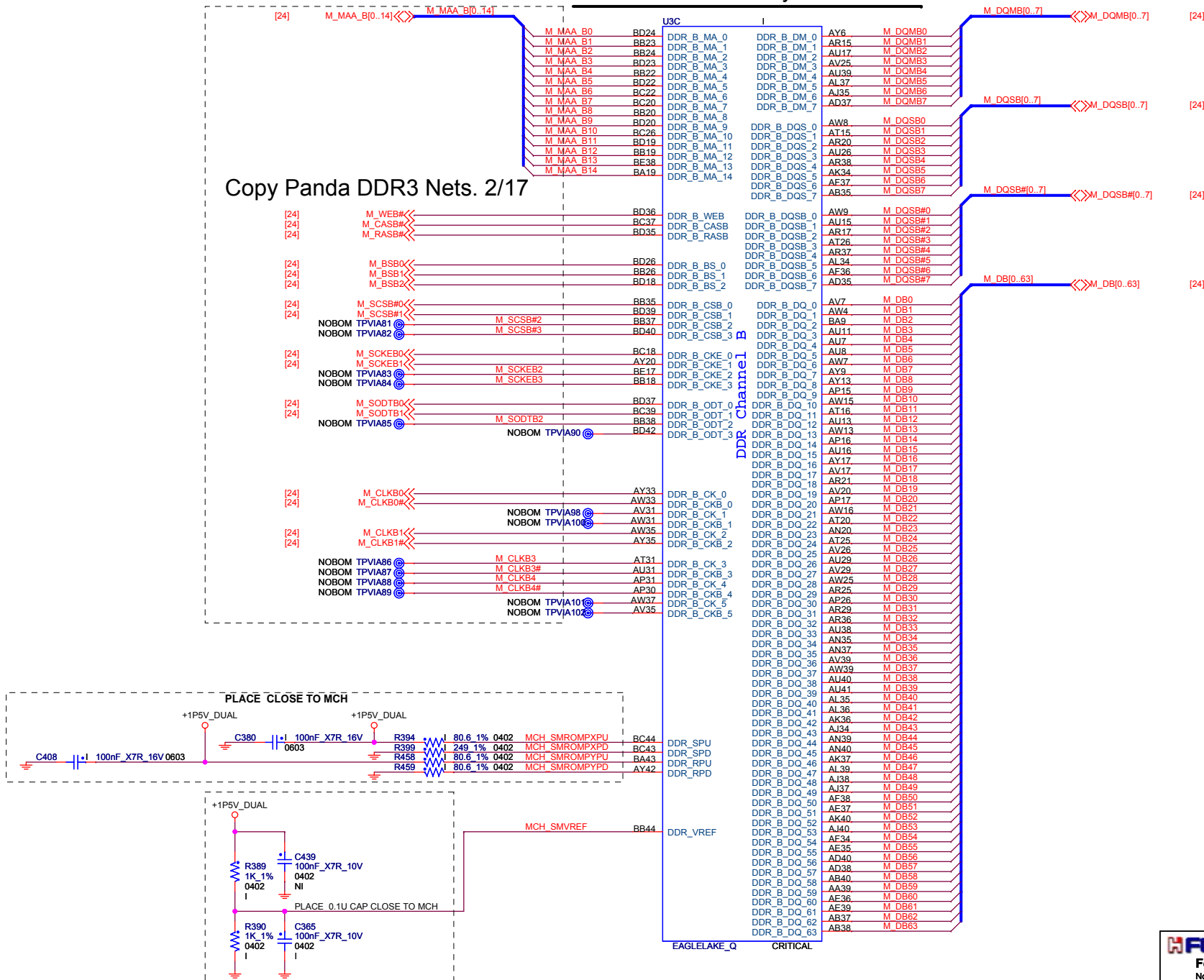


## DDR3 DRAMRSTB For ICH 10 Corporate Only

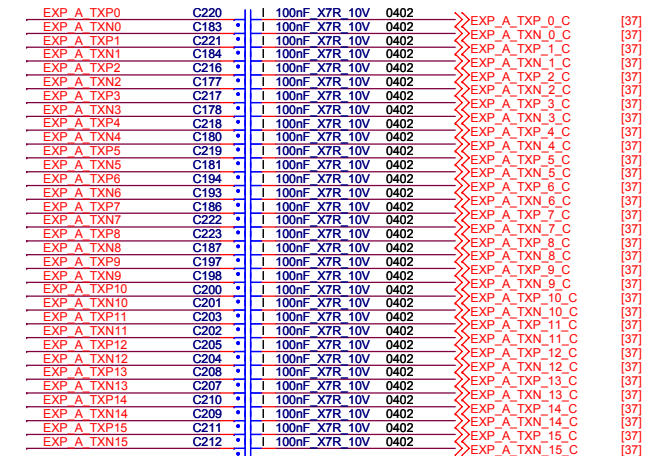


# MCH-DDR3 Memory Channel B

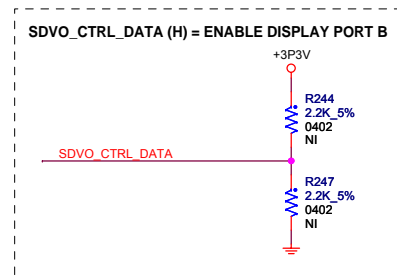
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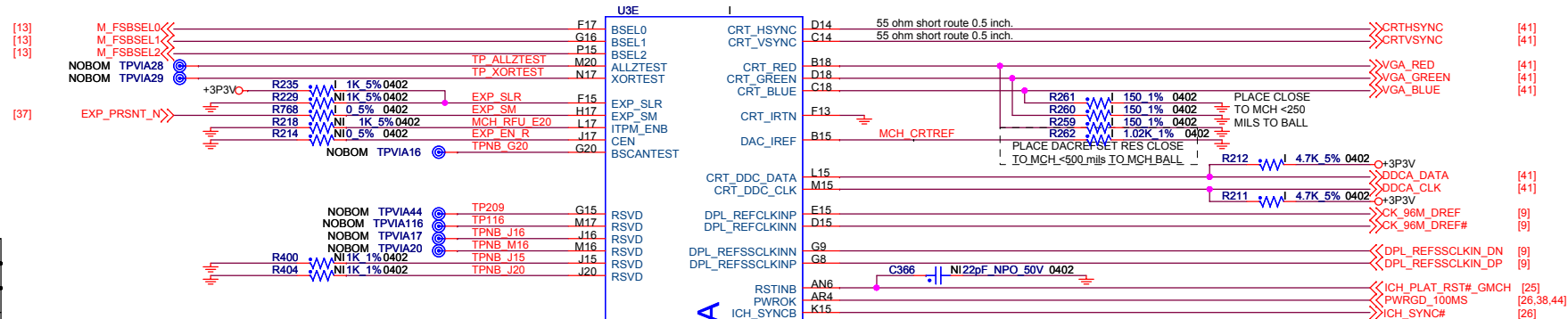
**AC coupling caps must be placed within .250" of PCI x16 Graphics connector**



	H	L	DESCRIPTION
MCH_MTYPE	NOT IN PRIMARY SLOT	PRIMARY SLOT	PRIMARY_PEG_PRESENCE
DUALX8 ENABLE	1X16 PCIE PORT ENABLE	2X8 PCIE PORT ENABLE	PCIE PORT BIFURCATION

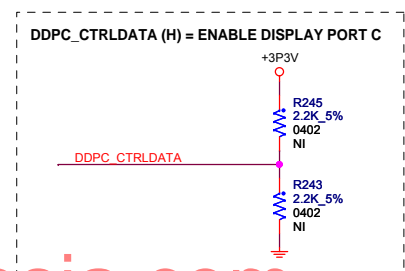
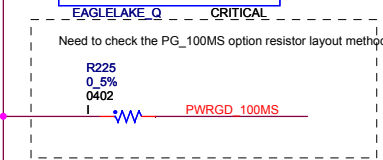
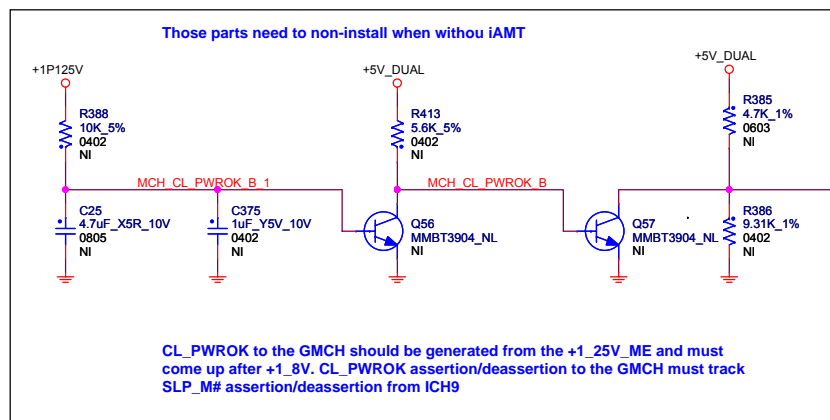
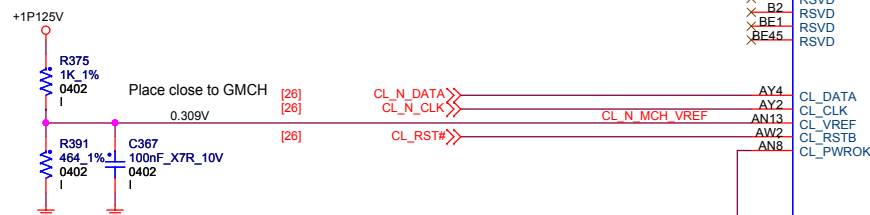


## MCH-VGA/MISC



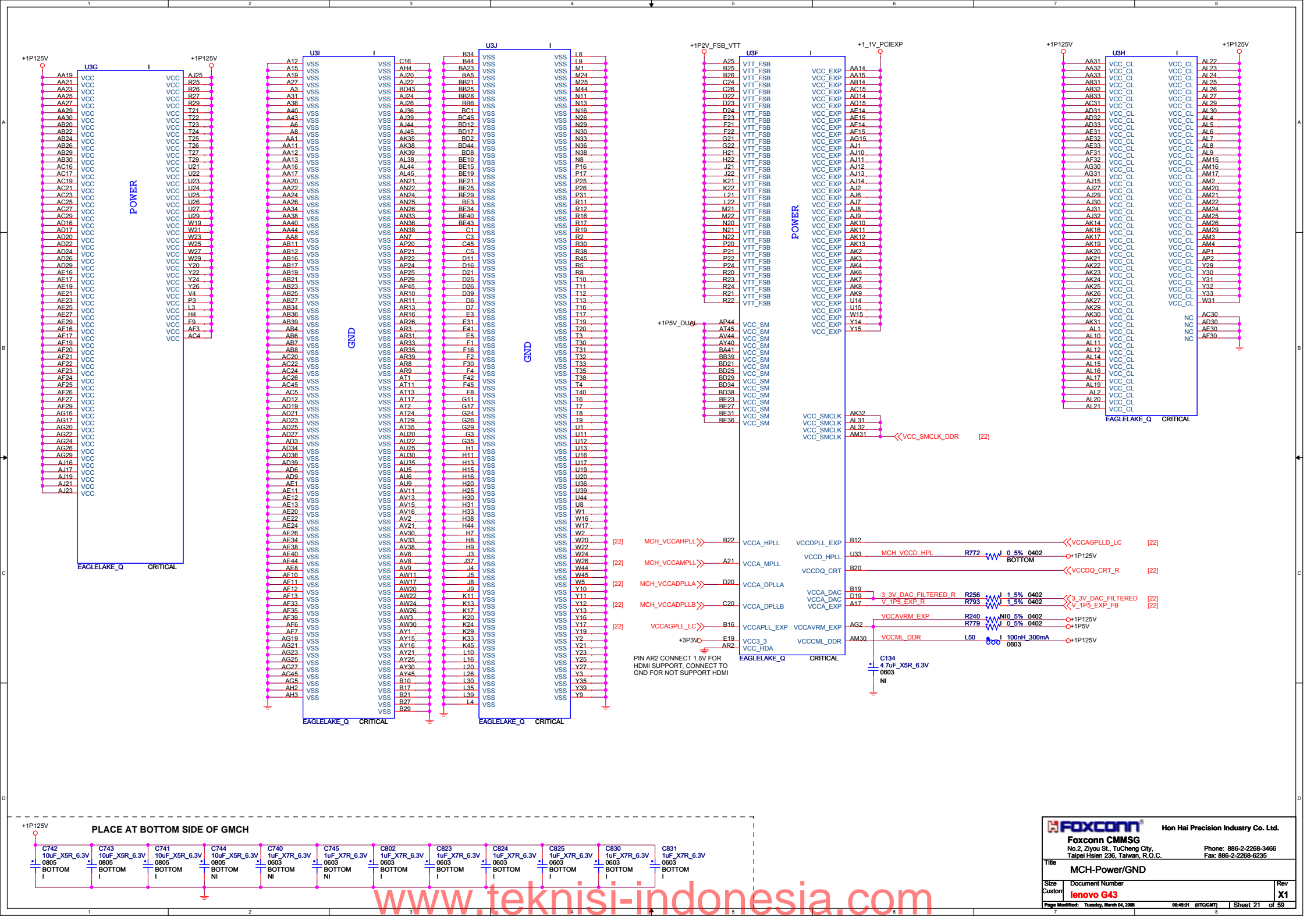
BSEL TABLE			
2	1	0	FSB FREQUENCY
0	0	0	266 MHZ (1067)
1	0	0	333 MHZ (1333)

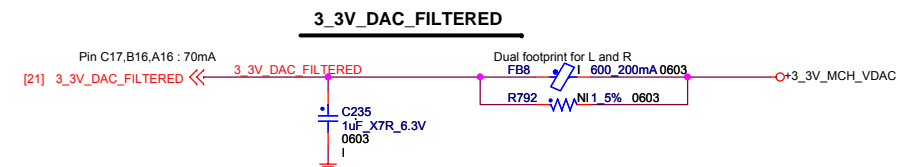
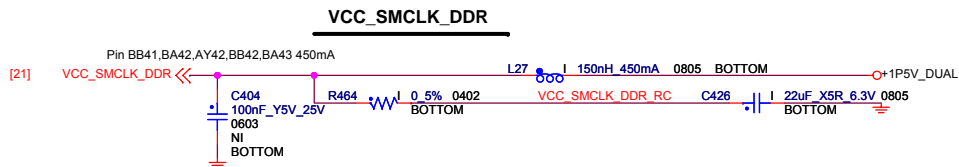
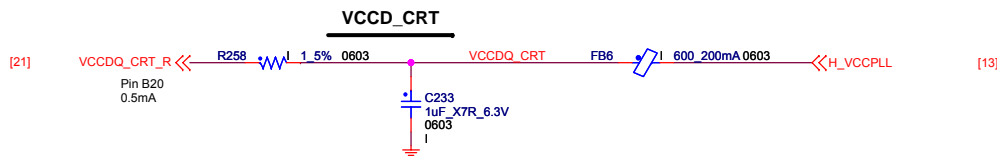
	H	L	DESCRIPTION
EXP_SLR	NORM ●	REVERSE	PCIe LANE NORMAL
EXP_EN_R	ENABLE ●	DISABLE	TLS CONFIDENTIALITY
MCH_SM	ENABLE ●	DISABLE	CONCURRENT PCIe PORT (ENABLE SDVO AND PCIe)



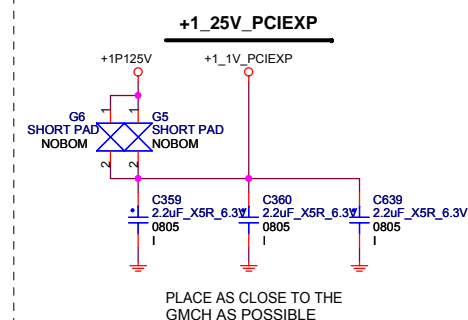
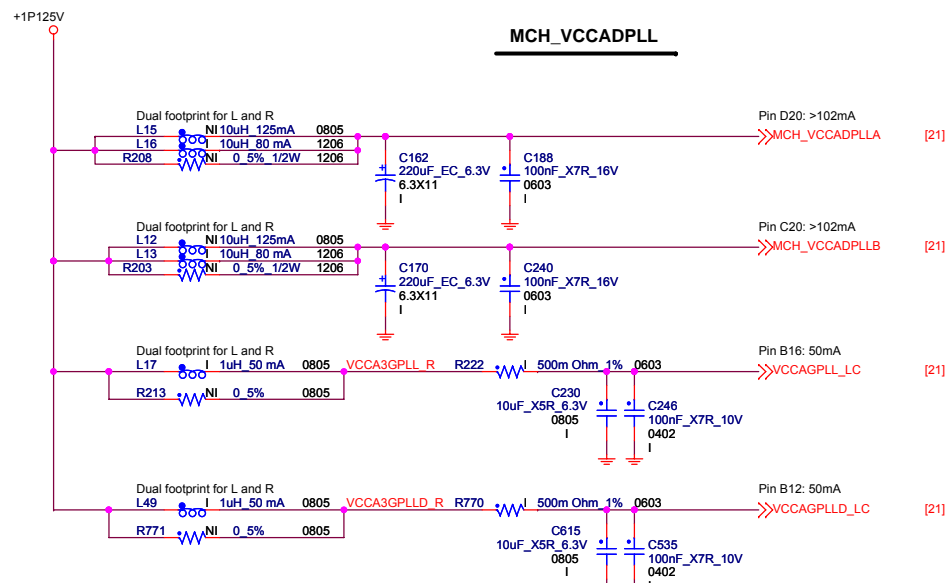
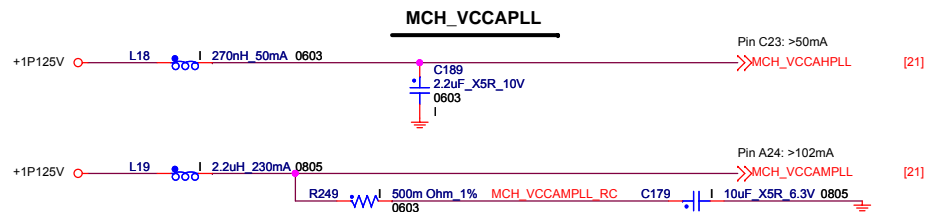
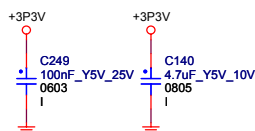
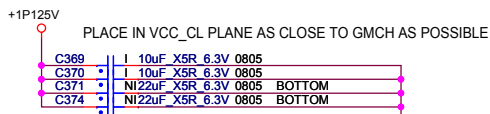
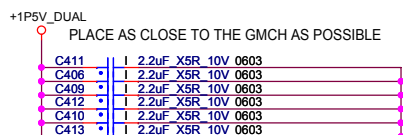
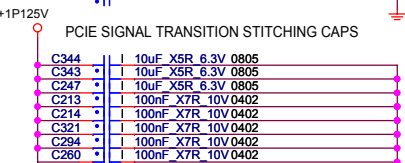
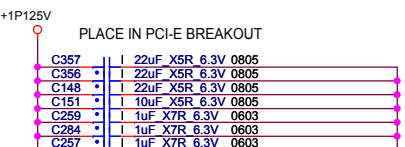
### Integrated TPM Straps (DG\_V1.3 : Figure12-10)

	Low	High	Float
ENABLE	ITPM_EN(GMCH.L17)	TPM_PP(ICH.C12) SPI_MOSI(ICH.C26)	
DISENABLE	TPM_PP(ICH.C12)		ITPM_EN(GMCH.L17) SPI_MOSI(ICH.C26)





### DECOUPLING CAP



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**Foxconn CMMSG**  
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Phone: 886-2-2268-3466  
Fax: 886-2-2268-6235

Title: **MCH-Decoupling / Filter**

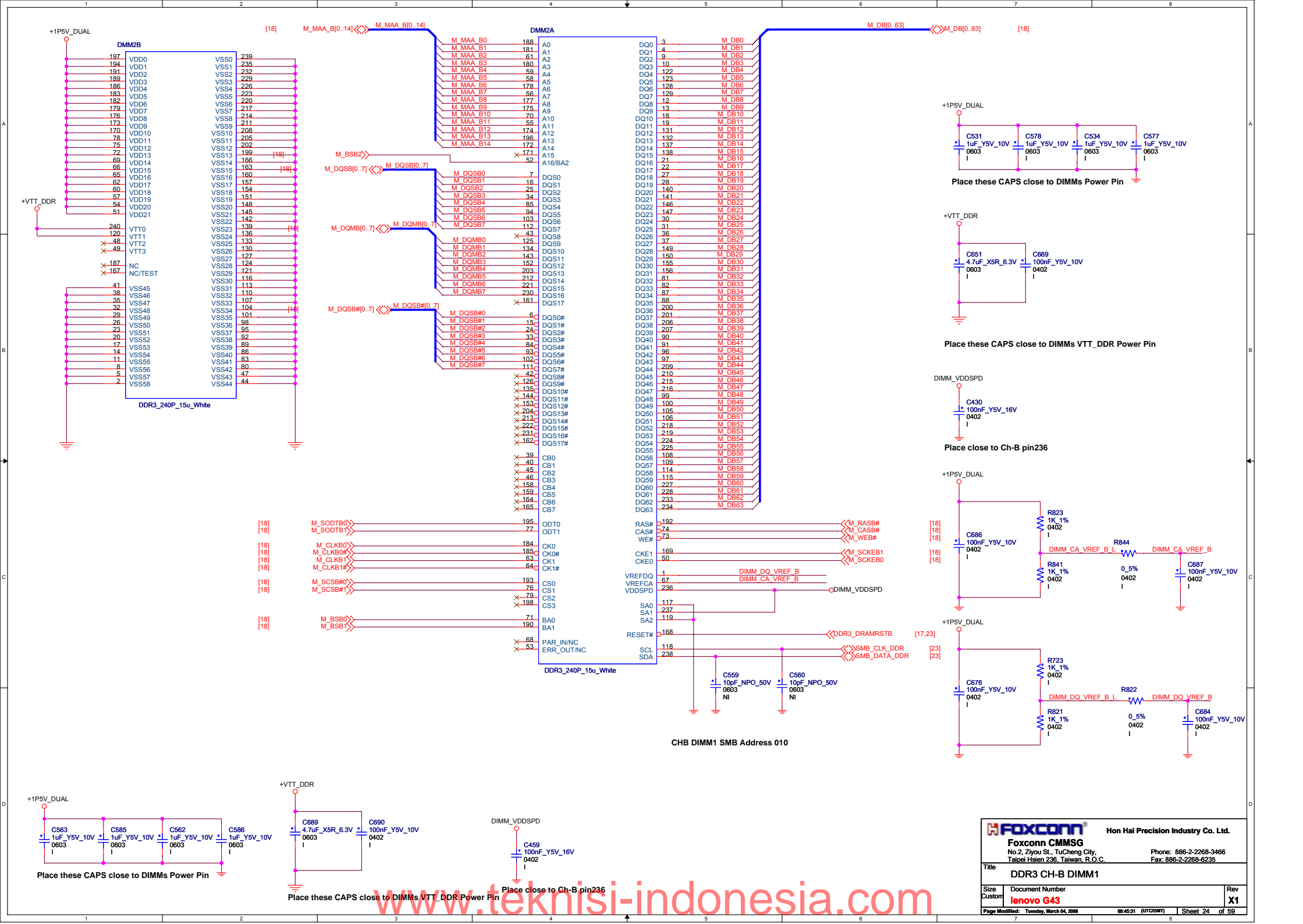
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Rev **X1**





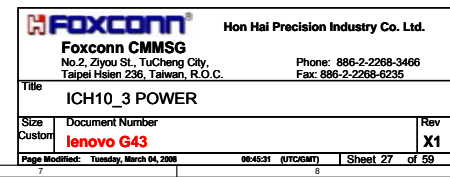




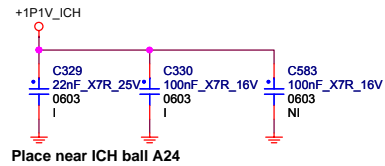




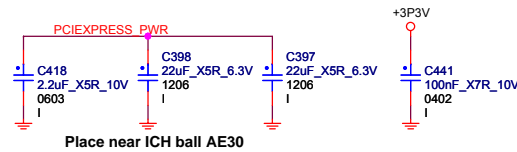
GND



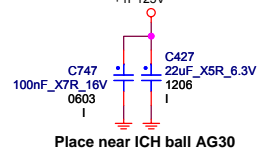
## ICH CORE



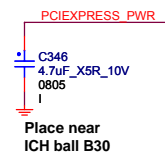
## PCI EXPRESS



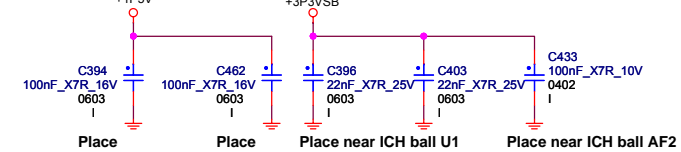
## DMI



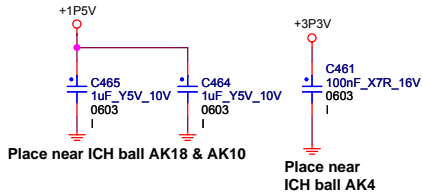
## GLAN



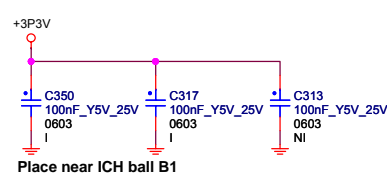
## USB



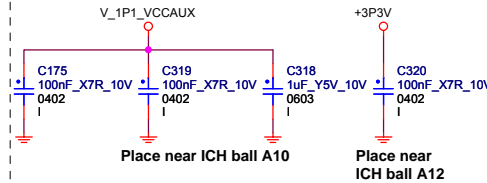
## SATA



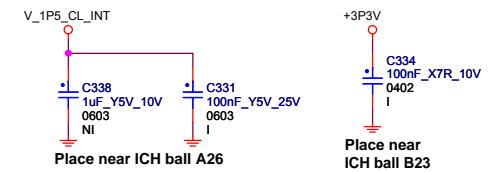
## PCI



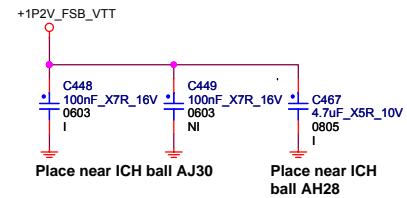
## GLAN



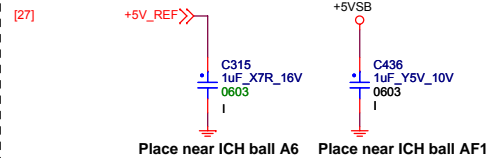
## CONTROL LINK



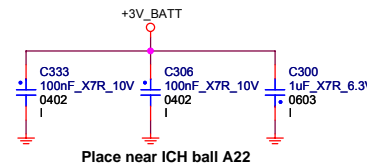
## CPU



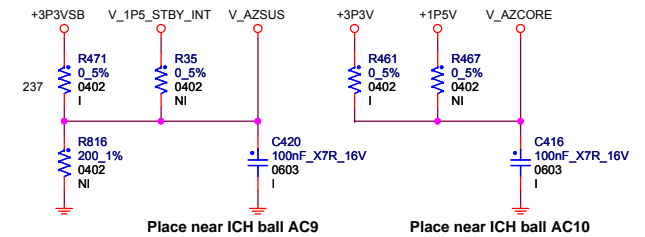
## 5V REFERENCE



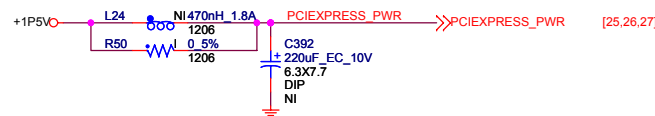
## RTC



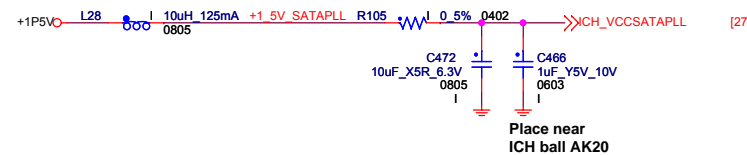
## AUDIO



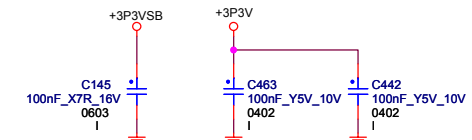
## PCI-E / VCCGLAN1\_5 FILTER



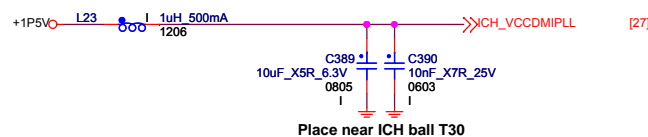
## SATA FILTER



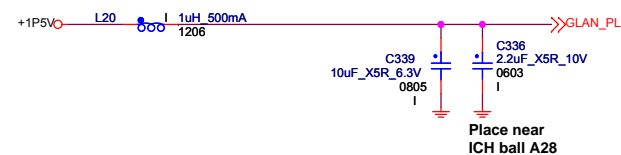
## Decoupling cap



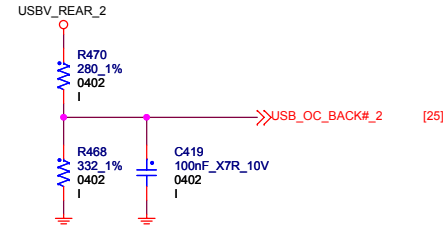
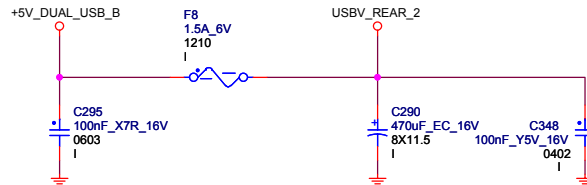
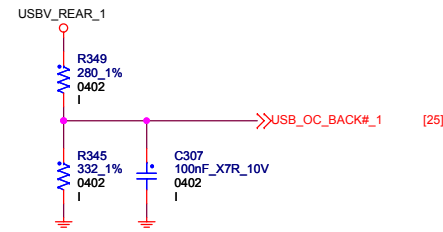
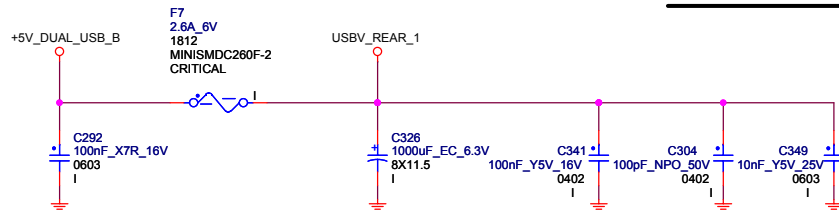
## DMI PLL FILTER



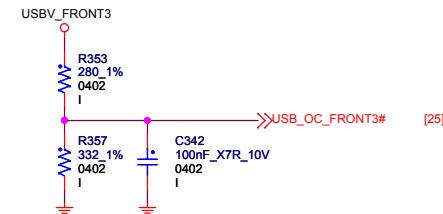
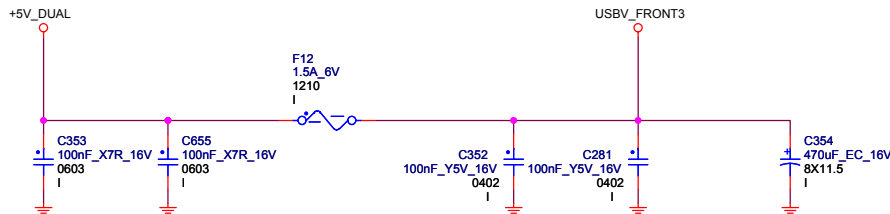
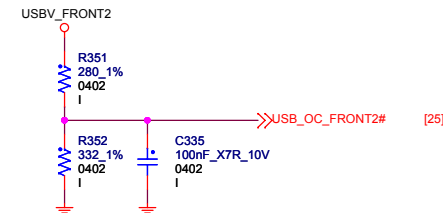
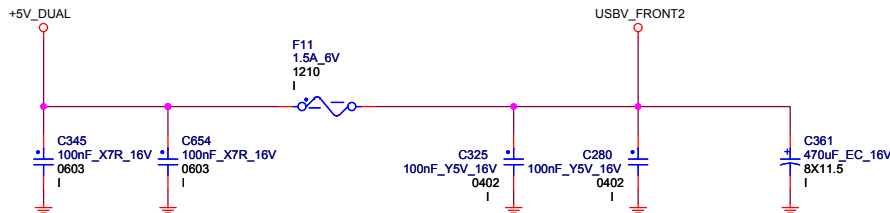
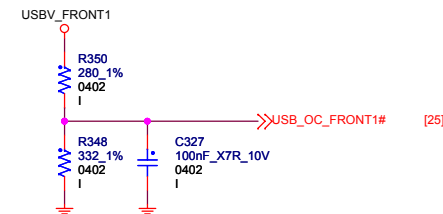
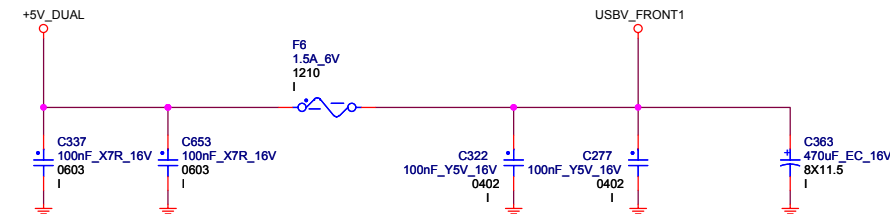
## GLAN FILTER




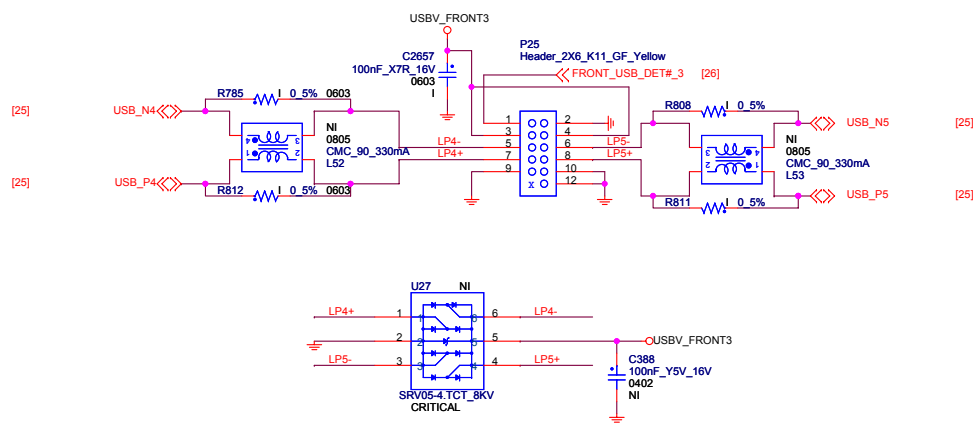
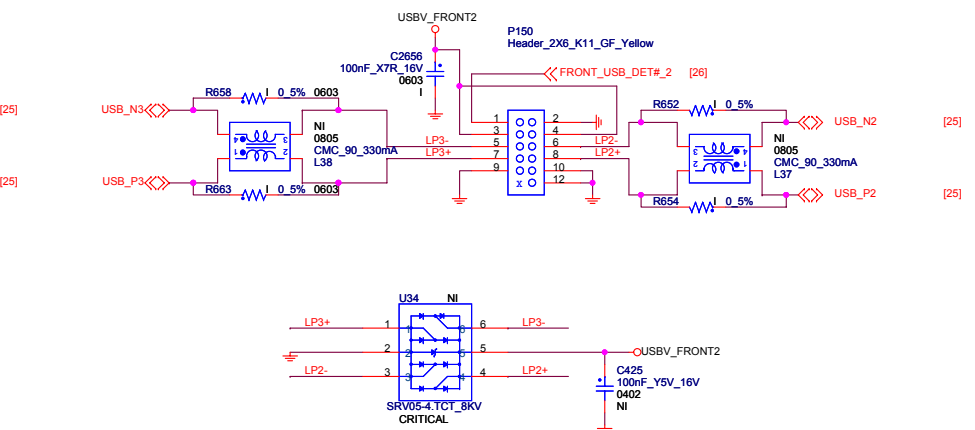
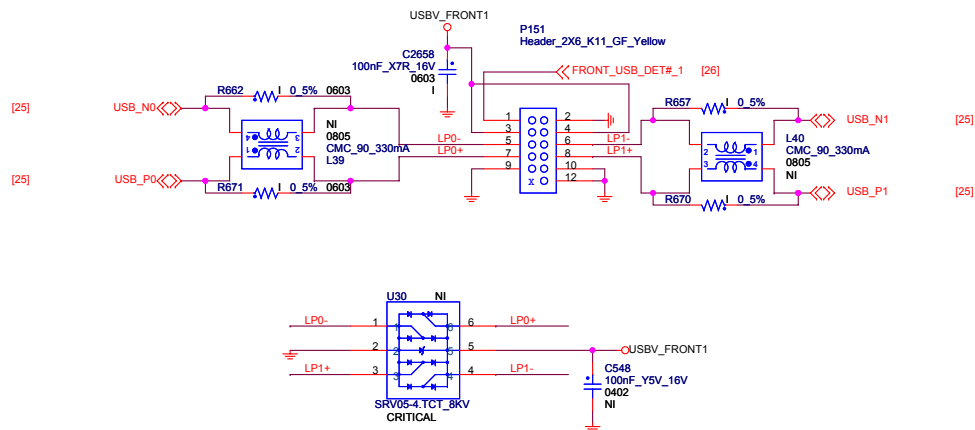
## REAR USB POWER



## FRONT USB POWER

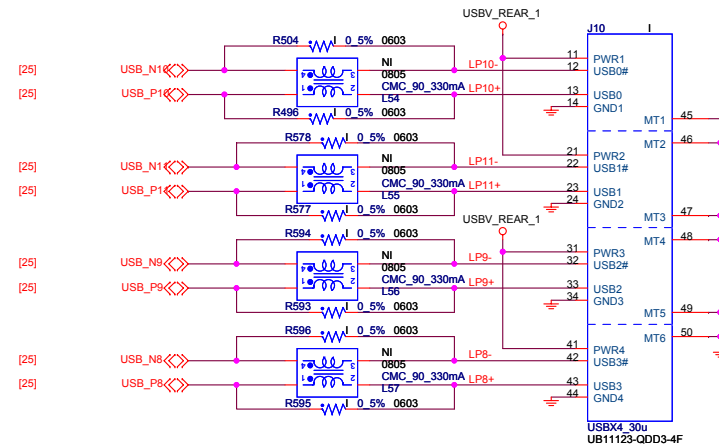


 <b>Foxconn CMMSG</b> No.2, Ziyou St., TuCheng City, Taipei Hsien 236, Taiwan, R.O.C.		<b>Hon Hai Precision Industry Co. Ltd.</b>  Phone: 886-2-2268-3466 Fax: 886-2-2268-6235	
Title <b>USB POWER</b>			
Size Custom	Document Number <b>lenovo G43</b>		Rev <b>X1</b>
Page Modified: Tuesday, March 04, 2008		08:45:30 (UTC+GMT)	Sheet 29 of 59

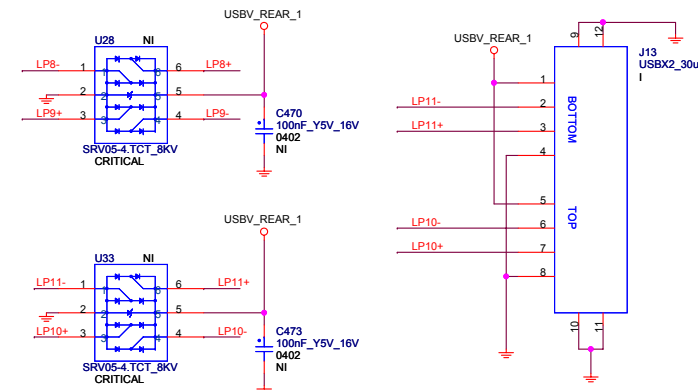


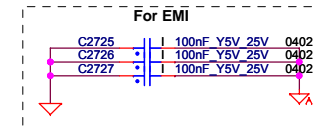
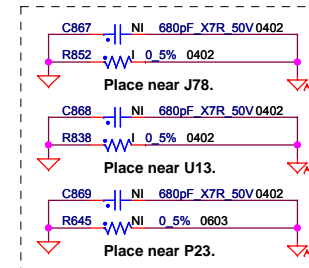
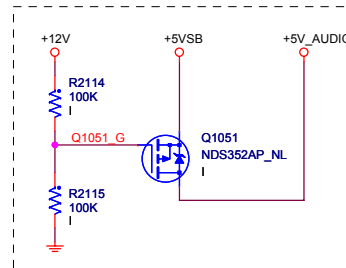
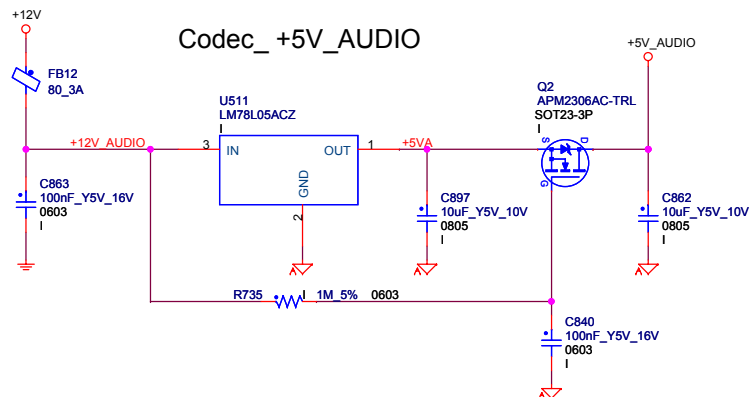
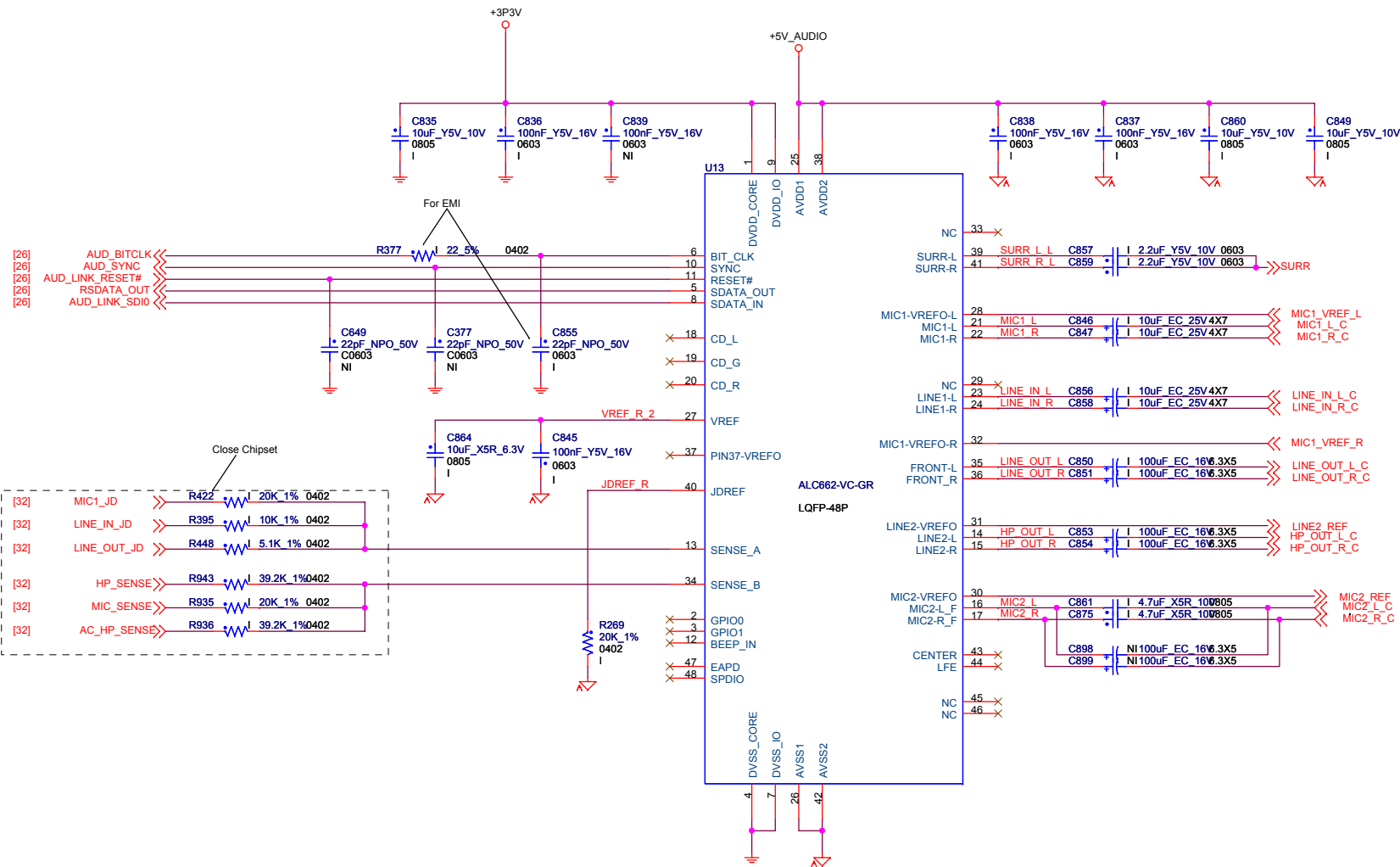
## REAR USB 4/2 Ports Co-layout

Ports 6, 7, 8, 9



## LAN USB ESD Component





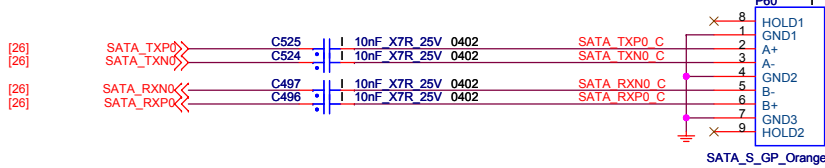




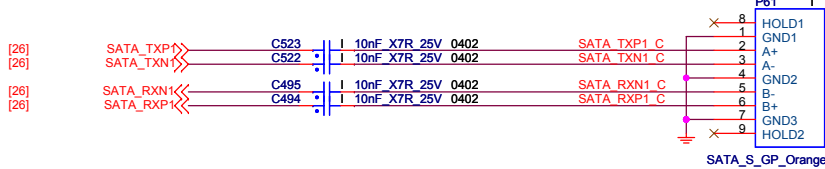


## SATA

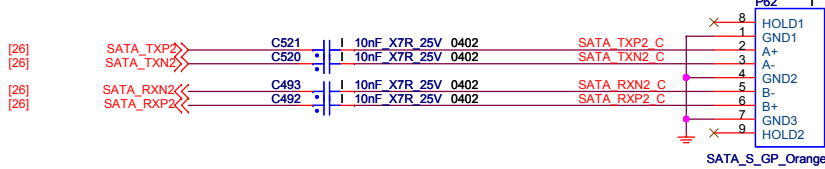
### SERIAL ATA 0 - 1ST CONTROLLER PRIMARY MASTER DARK BLUE



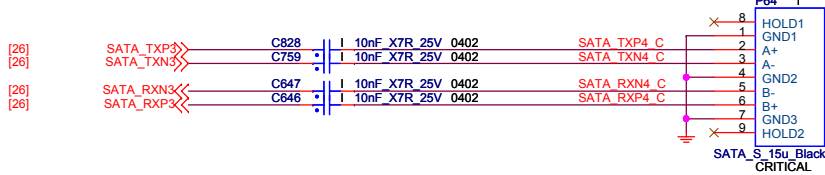
### SERIAL ATA 1 - 1ST CONTROLLER SECONDARY MASTER WHITE



### SERIAL ATA 2 - 1ST CONTROLLER PRIMARY SLAVE LIGHT BLUE



### SERIAL ATA 4 - 2ND CONTROLLER PRIMARY MASTER BLACK



Check ESATA Connector 2/22

### The Primary Hard drive will run off of SATA

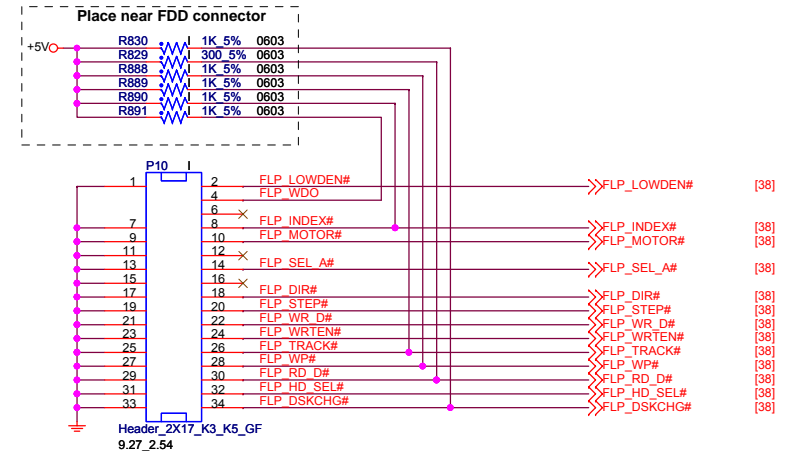
#### SERIAL ATA CAD NOTES:

- Serial ATA signals must be referenced to ground
- Minimize layer changes
- Do no route SATA signal under crystals, oscillators, clock synthesizers or magnetic devices.
- SATA spacing is the same as USB 2.0
- Maximum length of SATA is 3.8" with length mismatched to 20 mils within pair.

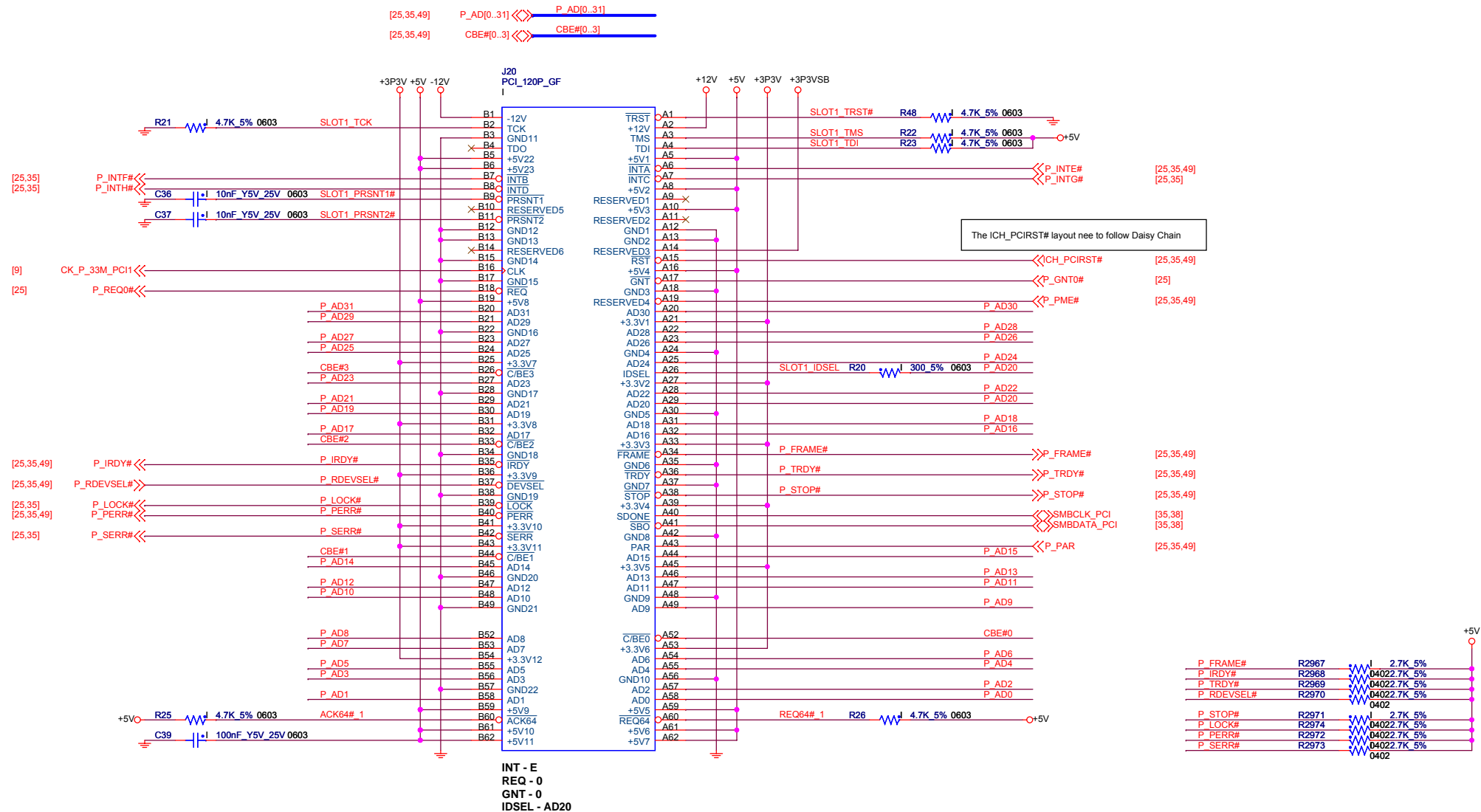
ESATA

## FDD

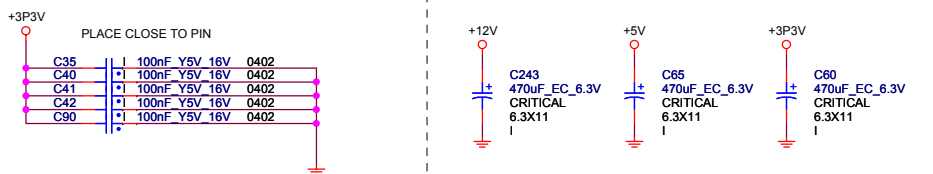
Board only supports one floppy drive.  
Must be a twisted floppy cable.



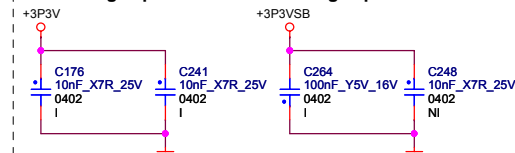
# PCI SLOT 1



## For PCI Slot 1,2

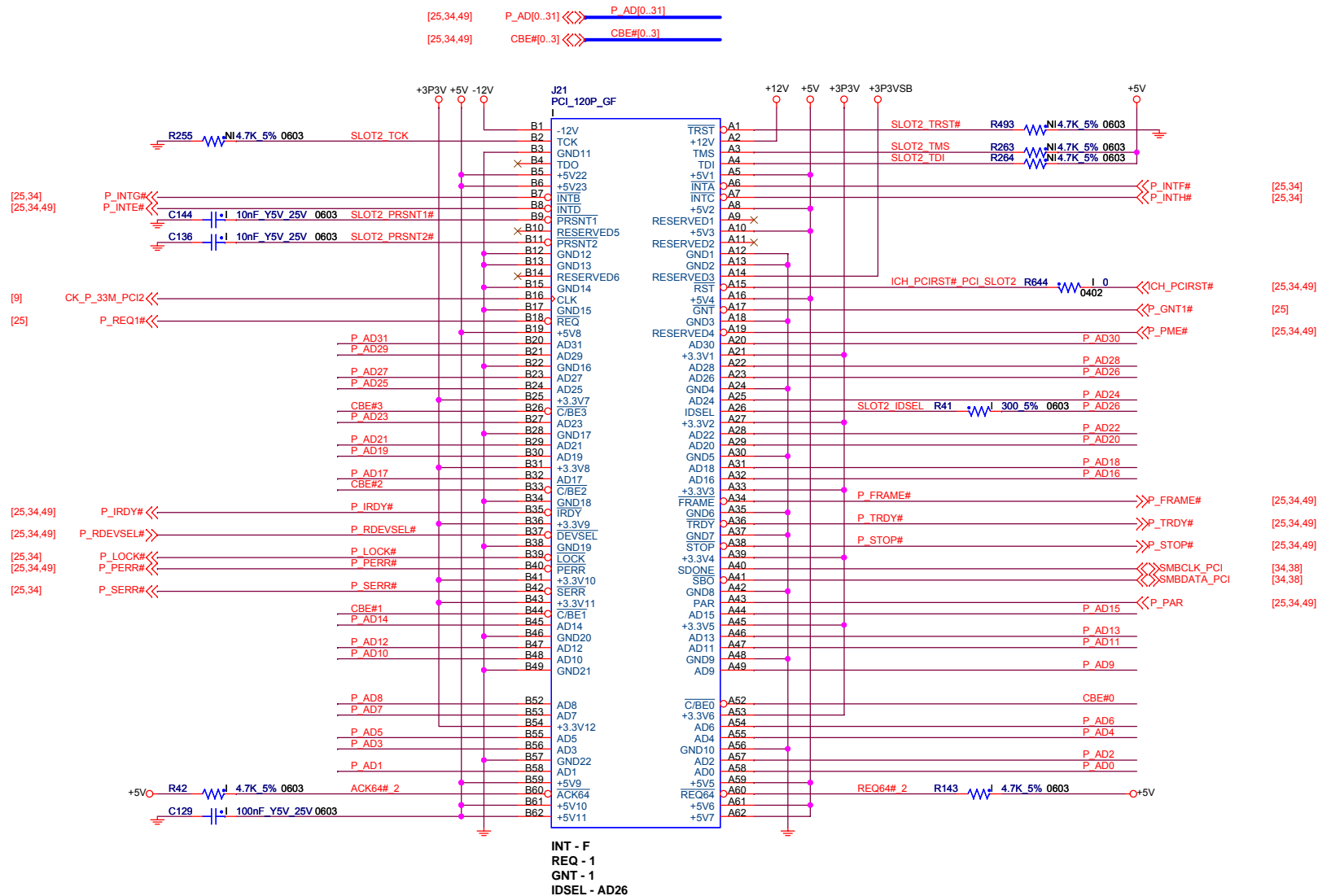


## Stitching caps

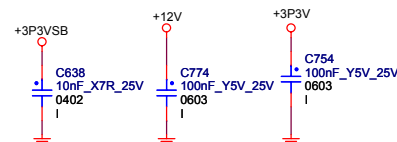


<b>FOXCONN</b> <b>Foxconn CMMSSG</b> No.2, Ziyou St., TuCheng City, Taipei Hsien 236, Taiwan, R.O.C.		<b>Hon Hai Precision Industry Co. Ltd.</b> Phone: 886-2-2268-3466 Fax: 886-2-2268-6235	
Title: <b>PCI 2.3 - PCI Slot 1</b>			
Size	Document Number	Rev	
Custom	<b>lenovo G43</b>	<b>X1</b>	
Page Modified: Tuesday, March 04, 2008		08:45:28 (UTC+GMT) Sheet 34 of 59	

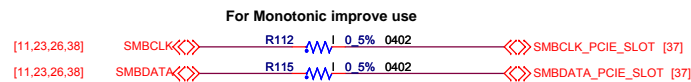
# PCI 2 SLOT



INT - F  
REQ - 1  
GNT - 1  
IDSEL - AD26



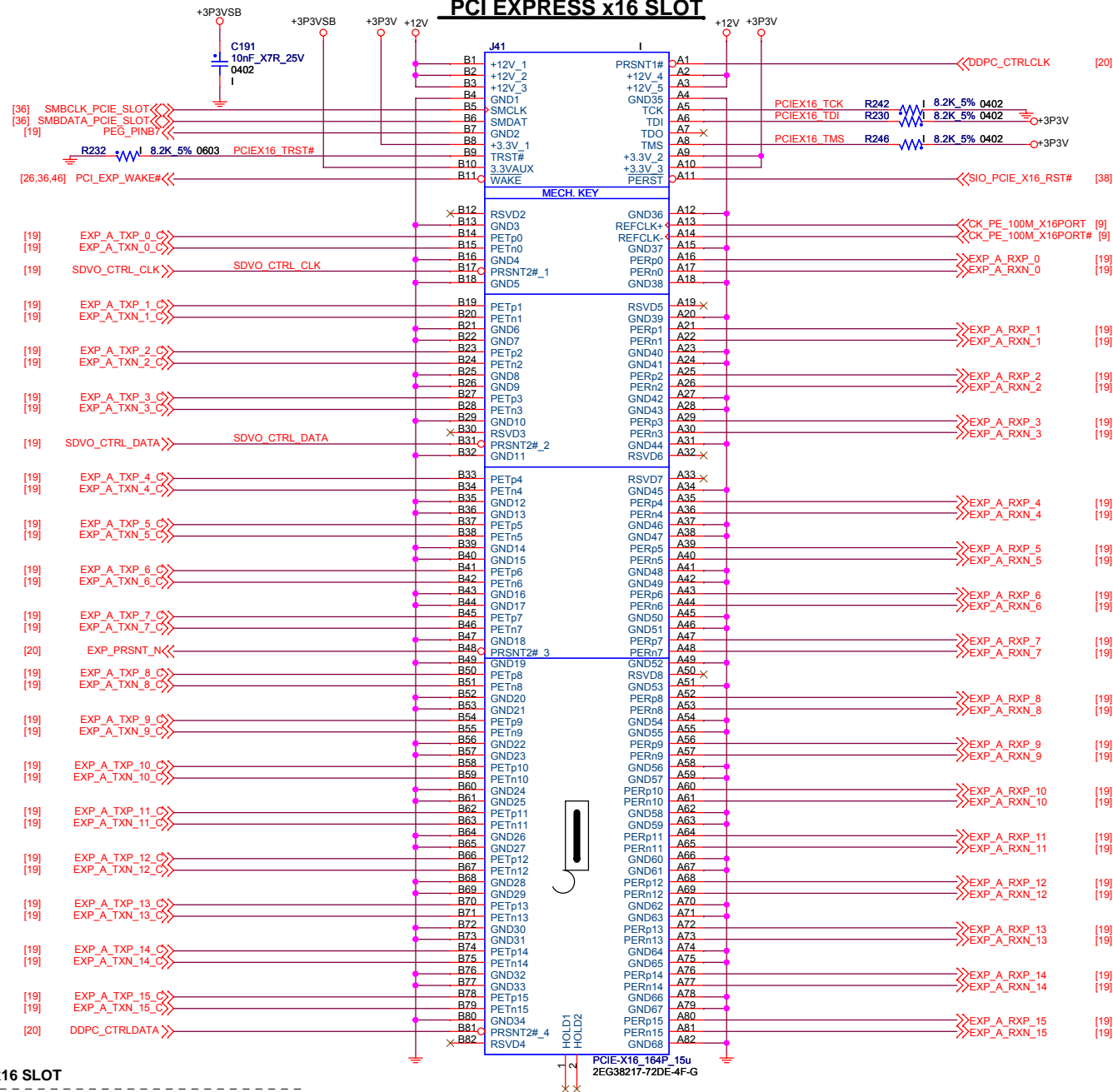
<b>FOXCONN</b>		Hon Hai Precision Industry Co. Ltd.	
<b>Foxconn CMMSG</b>		No.2, Ziyou St., TuCheng City, Taipei Hsien 236, Taiwan, R.O.C.	
Title		PCIEx4 Slot 1	
Size	Document Number	Rev	
Custom	<b>lenovo G43</b>	<b>X1</b>	
Page Modified: Tuesday, March 04, 2008		08:45:29 (UTC/GMT) Sheet 35 of 59	



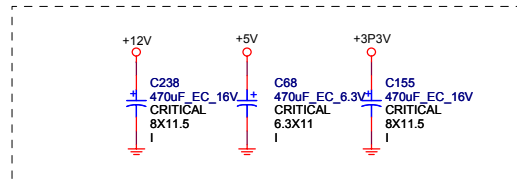
[11,23,26,38] SMBCLK  R112 | 0 5% 0402  SMBCLK\_PCIE\_SLOT [37]

[11,23,26,38] SMBDATA  R115 | 0 5% 0402  SMBDATA\_PCIE\_SLOT [37]

# PCI EXPRESS x16 SLOT



For PCIE x1 and x16 SLOT

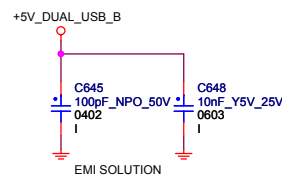
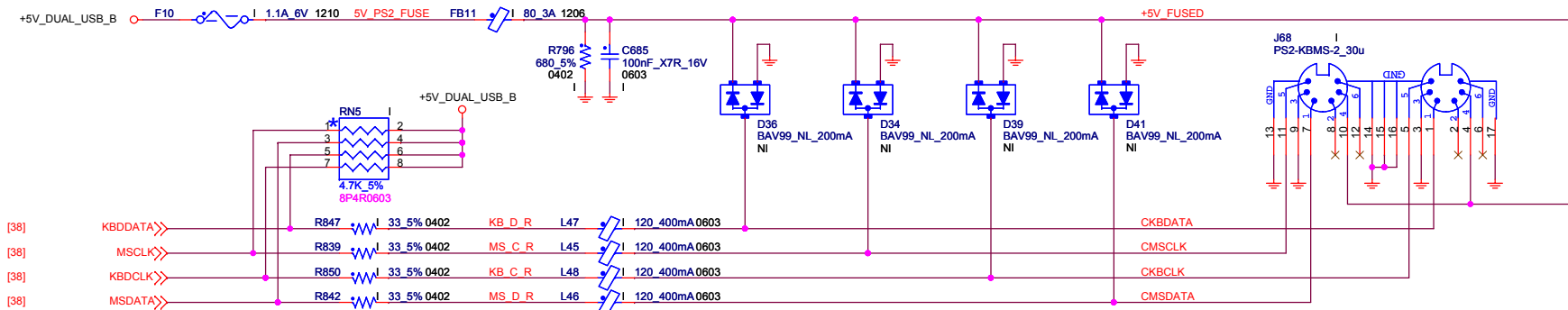






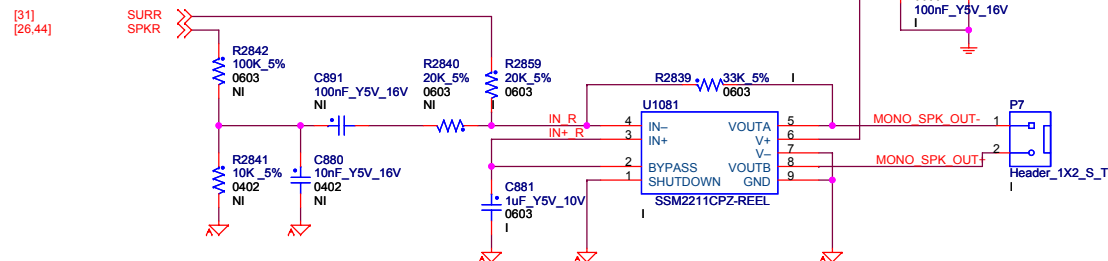
# KEYBOARD / MOUSE

The +5V\_FUSED power trace width must be 40 mils or greater

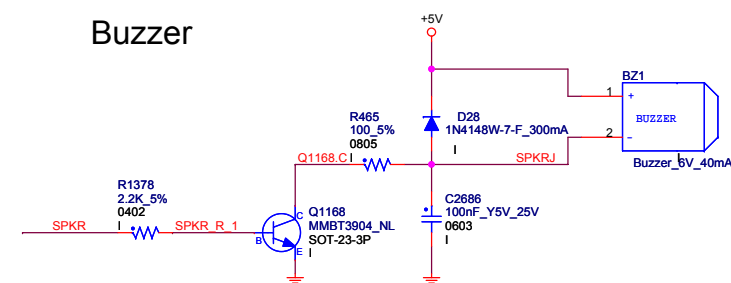


CKBCLK	C707	150pF NPO 25V 0402
CKBDATA	C712	150pF NPO 25V 0402
CMSDATA	C723	150pF NPO 25V 0402
CMSCLK	C724	150pF NPO 25V 0402

## Mono Out



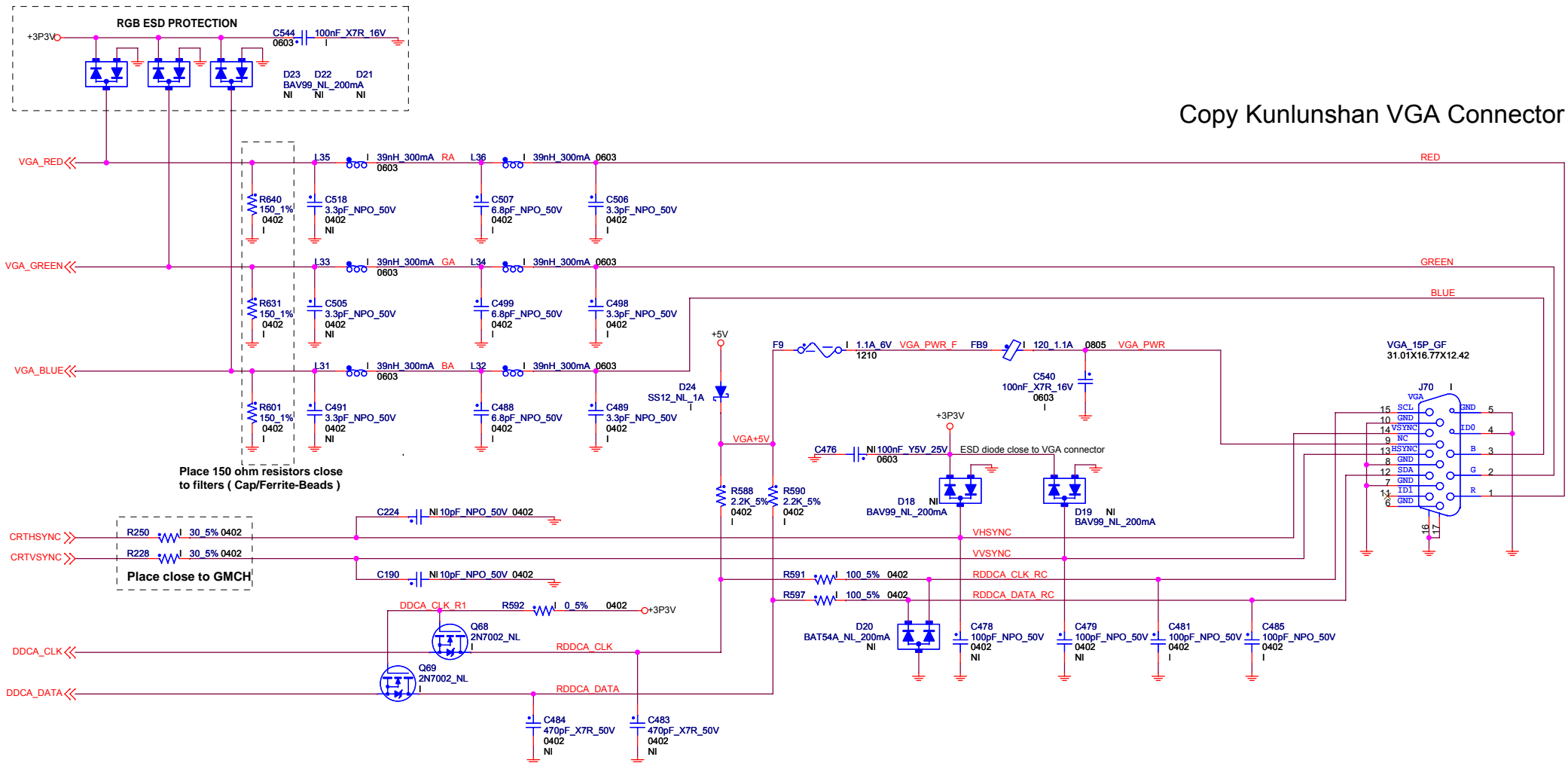
## Buzzer



<b>FOXCONN</b>		Hon Hai Precision Industry Co. Ltd.	
<b>Foxconn CMMSG</b>		No.2, Ziyou St., TuCheng City, Taipei Hsien 236, Taiwan, R.O.C.	
Title		PS2 KB/MS, Mono Out	
Size	Document Number	Rev	
Custom	lenovo G43	X1	
Page Modified: Tuesday, March 04, 2008		00:45:39 (UTC+08) Sheet 40 of 59	

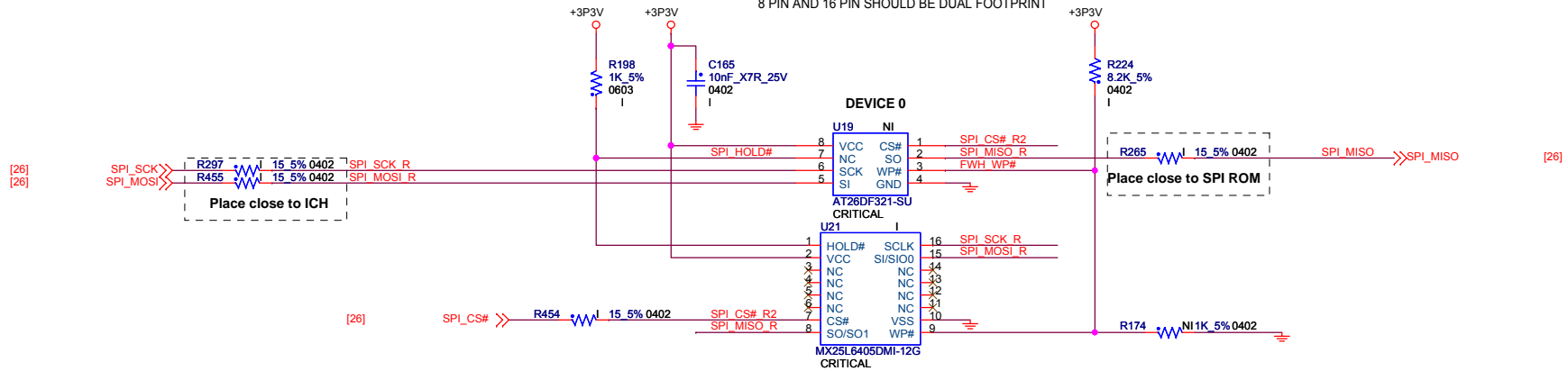


# Copy Kunlunshan VGA Connector



## SPI ROM

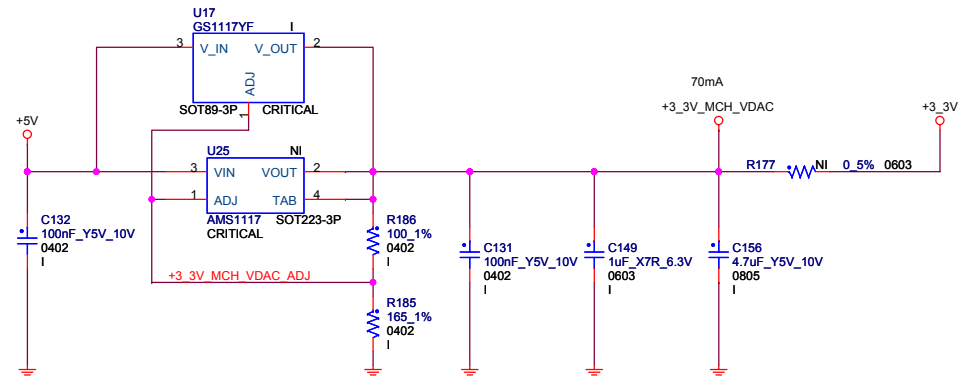
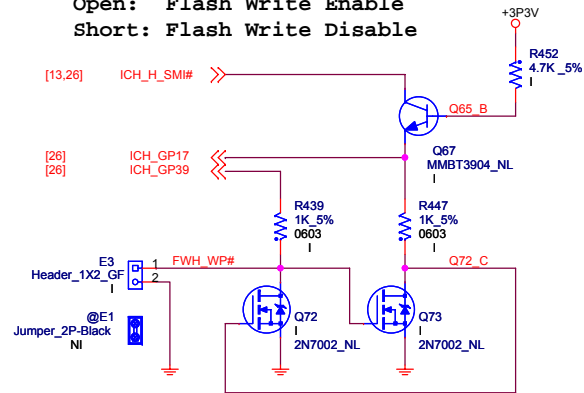
8 PIN AND 16 PIN SHOULD BE DUAL FOOTPRINT



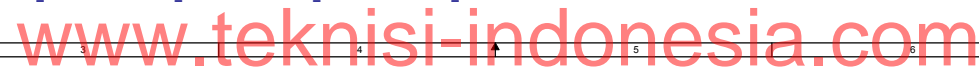
Poto using Socket

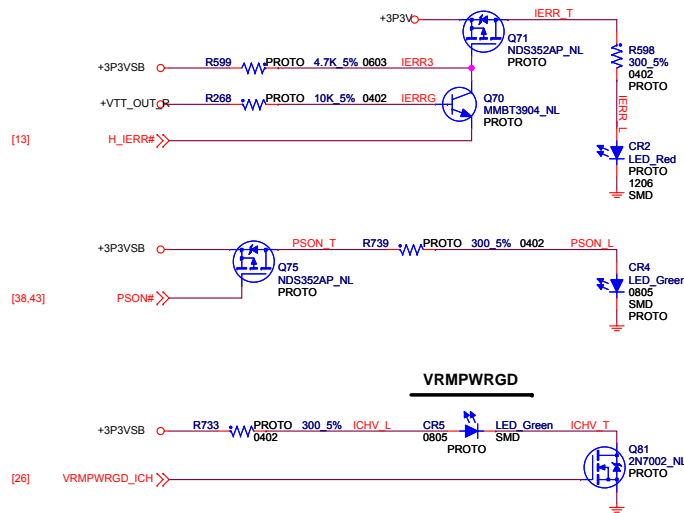
## BIOS WRITE PROTECT

Open: Flash Write Enable  
Short: Flash Write Disable



## Connector is long latch ?



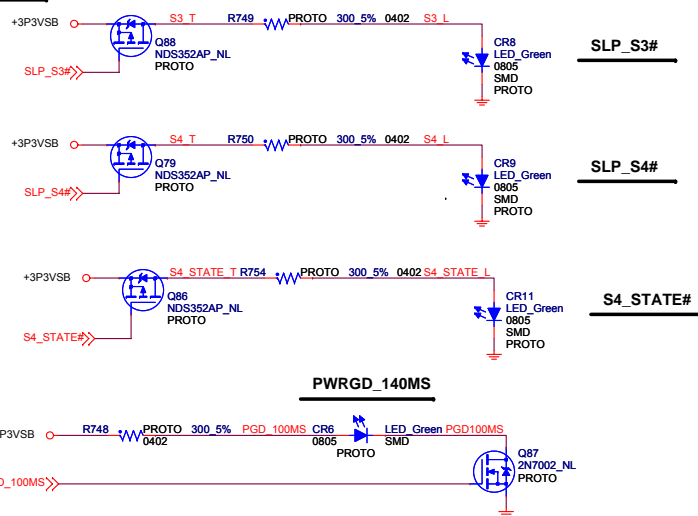
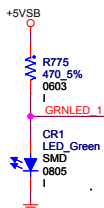


## PCA LED For Debug Only

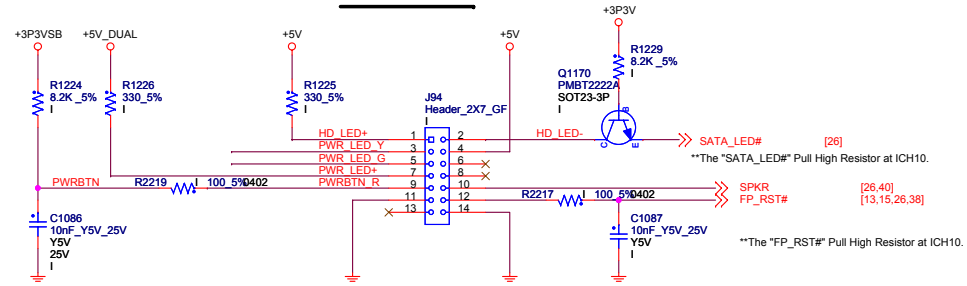
### IERR

### PSON#

### +5V\_AUX LED



## Front Panel

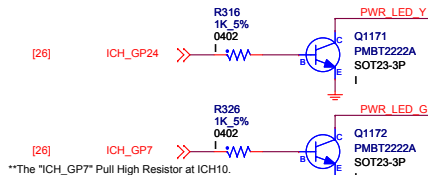


### 3 Pin LED Status

- S0 (Steady Green)
- S1 (Green Blinking 1Hz/S)
- S3 (Steady Yellow)
- S4/S5 (Off)

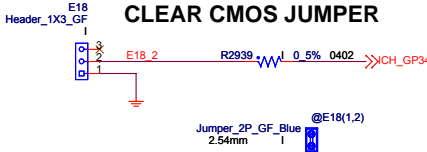
### 2 Pin LED Status

- S0 (Steady Green)
- S1/S3 (Blinking 1Hz/S)
- S4/S5 (Off)

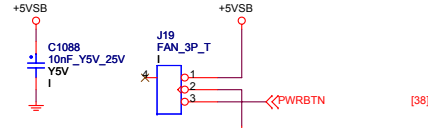


\*\*The "ICH\_GP7" Pull High Resistor at ICH10.

## CLEAR CMOS JUMPER

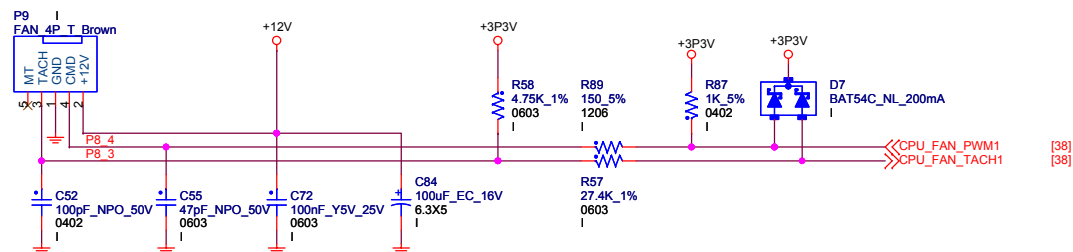


## FRISW

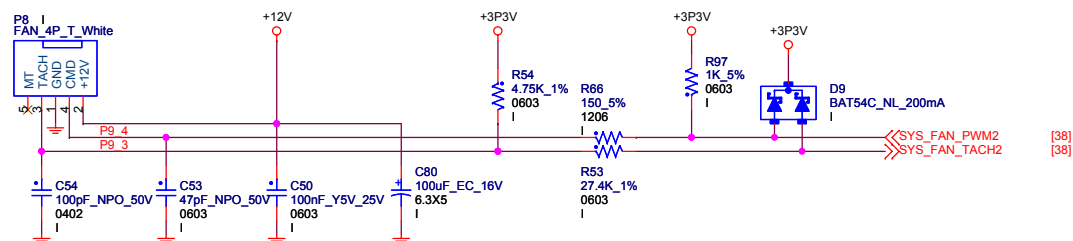


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Title		PCA LED Circuit	
Size	Document Number	Rev	
Custom	Lenovo G43	X1	
Date Modified: Tuesday, March 04, 2008		09:45:29 (UTC+8)   Sheet 44 of 59	

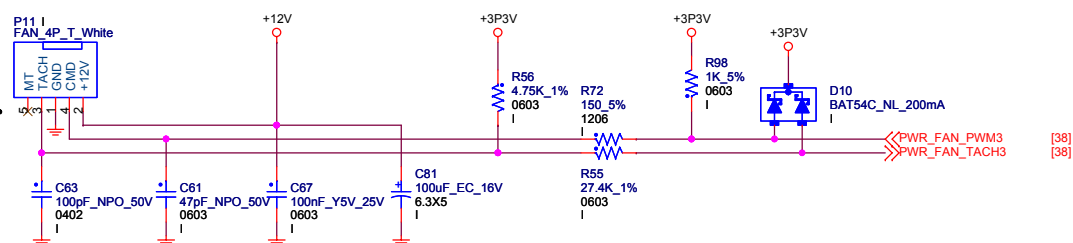
**Color: Brown**



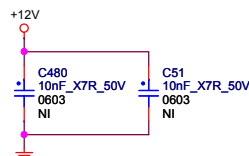
**Color: White**



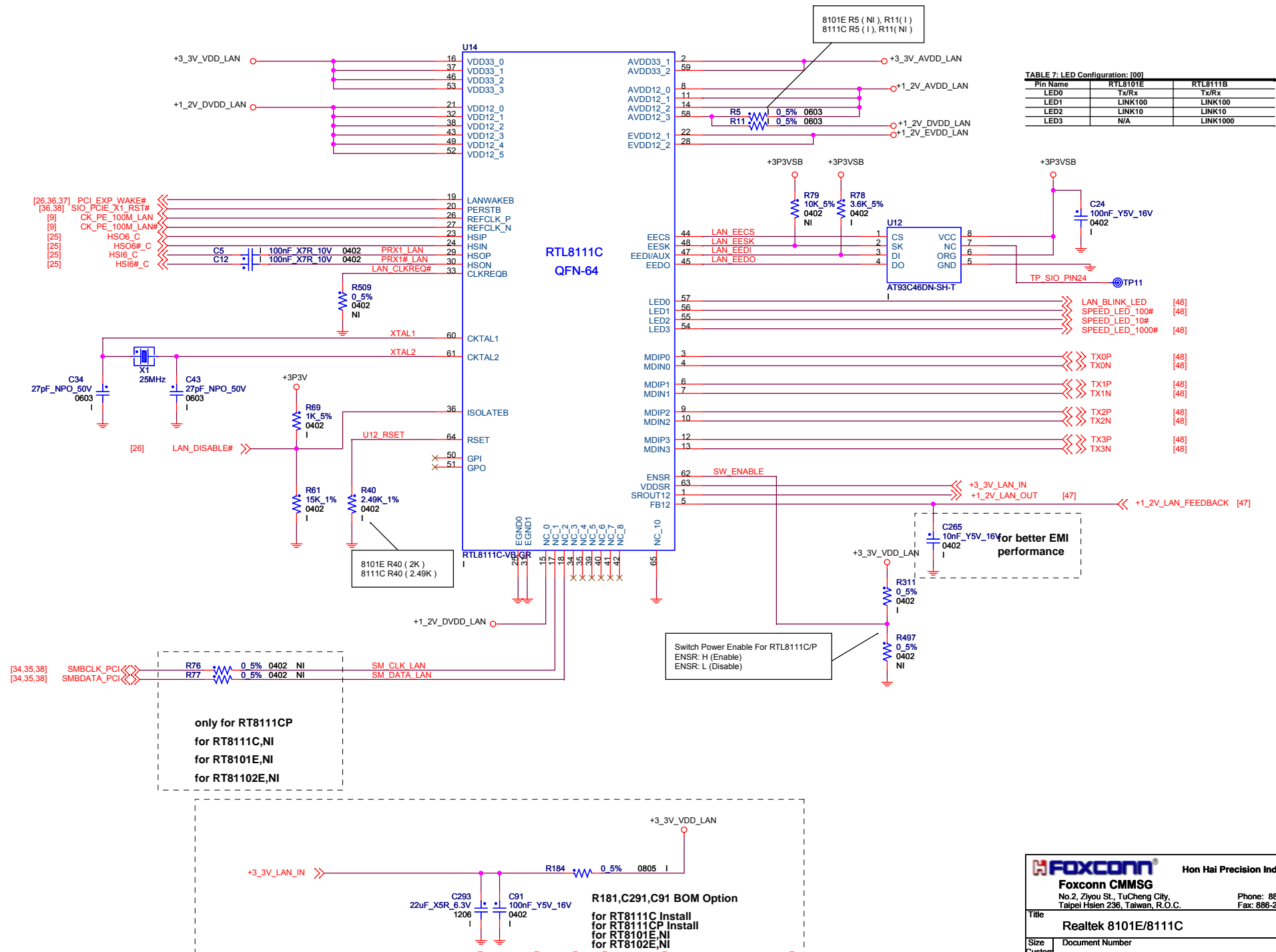
**Color: White**



**For EMI, add 2 .01uF  
Capacitors on +12V.**



## PCIE X1 Gigabit LOM - RTL8111C



# PCIE X1 Gigabit LOM Power

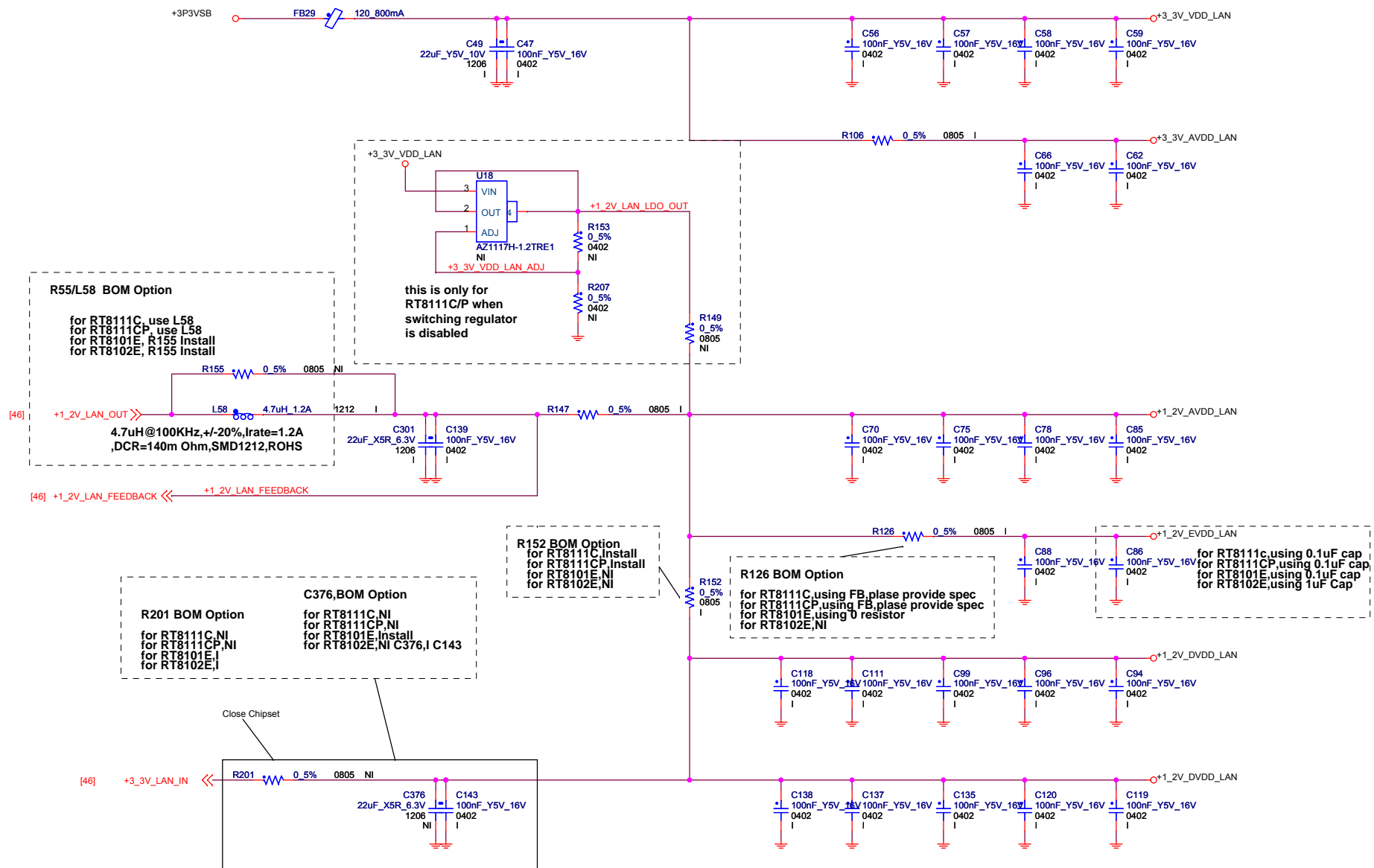


TABLE 8: Realtek LAN Power Rails

Power Rail	RTL8111B	RTL8101E	RTL8111C
+3.3V AVDD LAN	3.3V	3.3V	3.3V
+1.8V AVDD LAN	1.8V	1.8V	1.2V
+1.8V EVDD LAN	1.8V	1.8V	1.2V
+1.5V DVDD LAN	1.5V	1.5V	1.2V

**FOXCONN®** Hon Hai Precision Industry Co. Ltd.

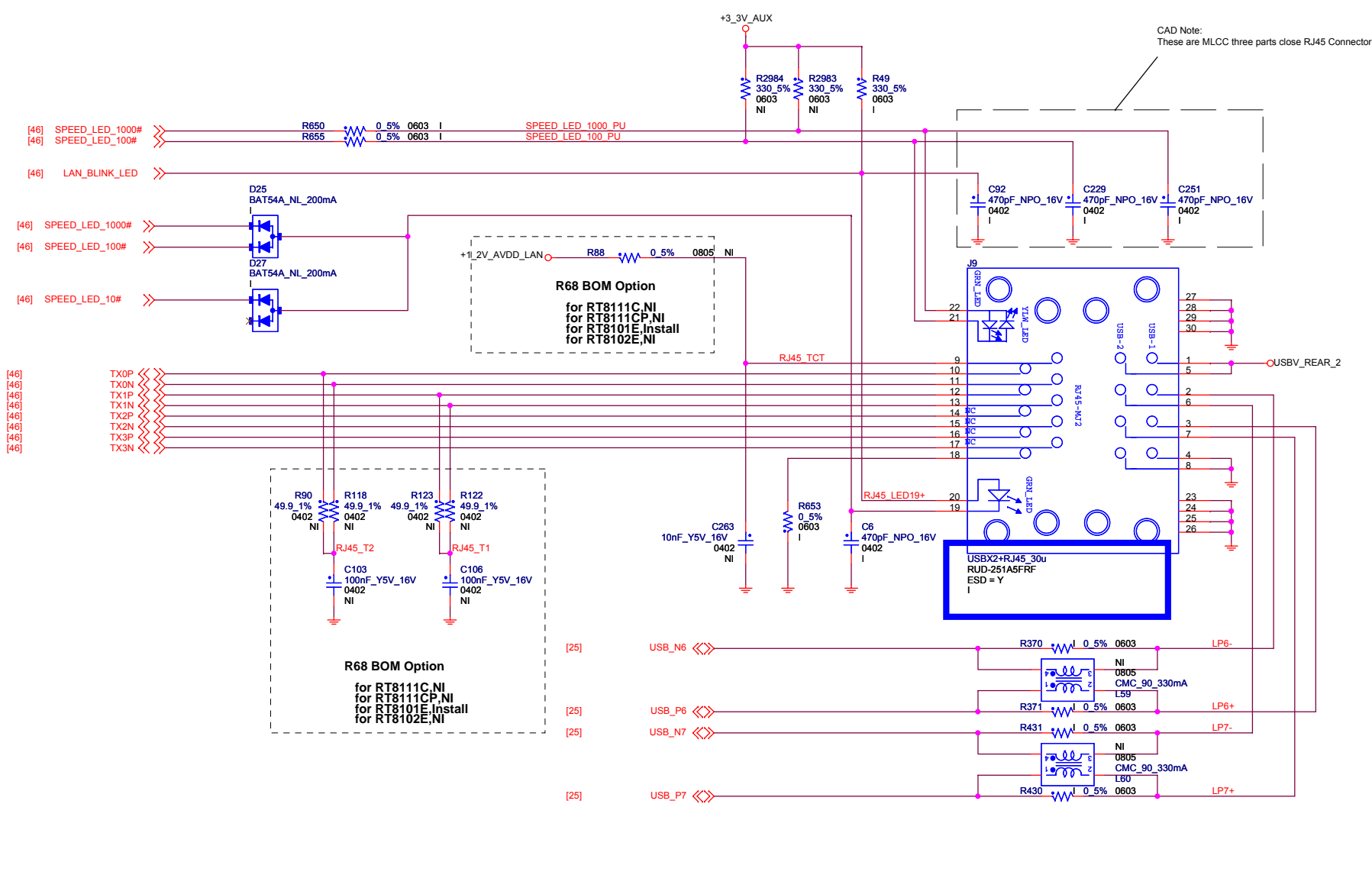
**Foxconn CMMSG**  
No.2, Ziyu St., TuCheng City,  
Taipei Hsien 236, Taiwan, R.O.C.

Phone: 886-2-2268-3466  
Fax: 886-2-2268-6235

Title: **Realtek 8101E/8111C Power**

Size: Custom Document Number: **lenovo G43** Rev: **X1**

Page Modified: Tuesday, March 04, 2008 00:45:39 (UTC+08) Sheet 47 of 59



CAD Note:  
These are MLCC three parts close RJ45 Connector

[46] SPEED\_LED\_1000#  
[46] SPEED\_LED\_100#  
[46] LAN\_BLINK\_LED  
[46] SPEED\_LED\_1000#  
[46] SPEED\_LED\_100#  
[46] SPEED\_LED\_10#

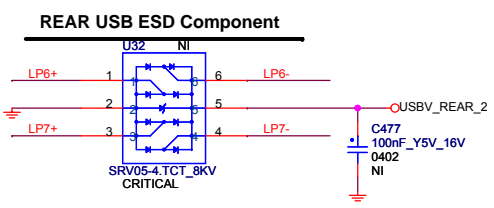
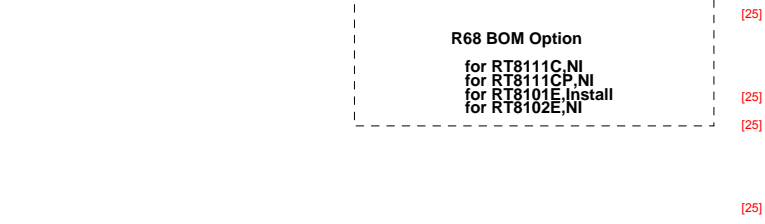


TABLE5: RJ-45 LED define(For Giga LAN)

	LEFT LED	RIGHT LED
	TRAFFIC_LED	SPD_LED
NO LINK CABLE		
10M LINK CABLE IN,NO DATA		
10M LINK CABLE IN,DATA I/O	+FLASH	
100M LINK CABLE IN ,NO DATA		
100M LINK CABLE IN,DATA I/O	+FLASH	
1G LINK CABLE IN,NO DATA		
1G LINK CABLE IN,DATA I/O	+FLASH	
S3,S4,S5		

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Title  
**RJ45, CaseOpen and Clear CMOS**

Size  
 Custom

Document Number  
**lenovo G43**

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 08:45:29 (UTC+GMT)

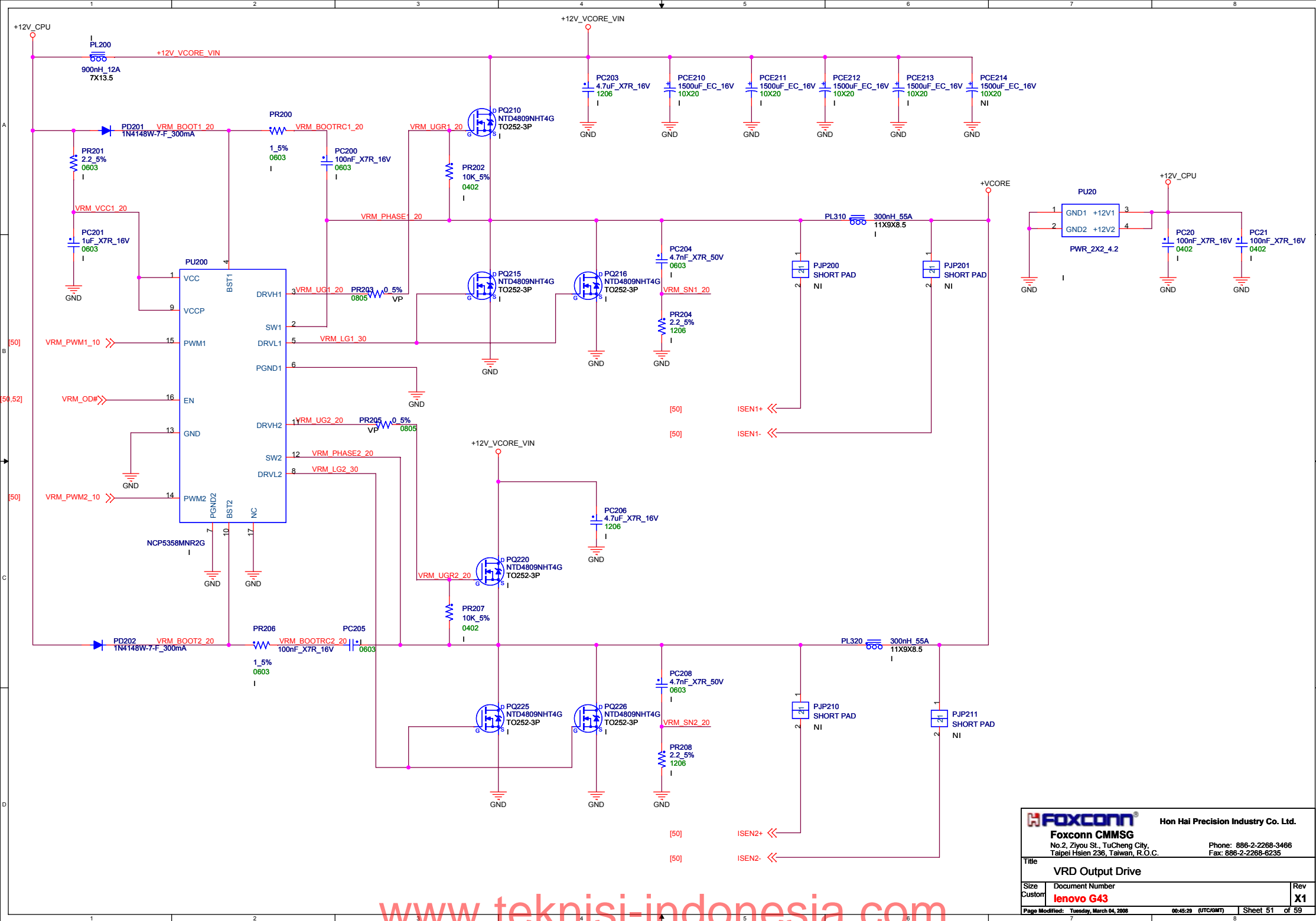
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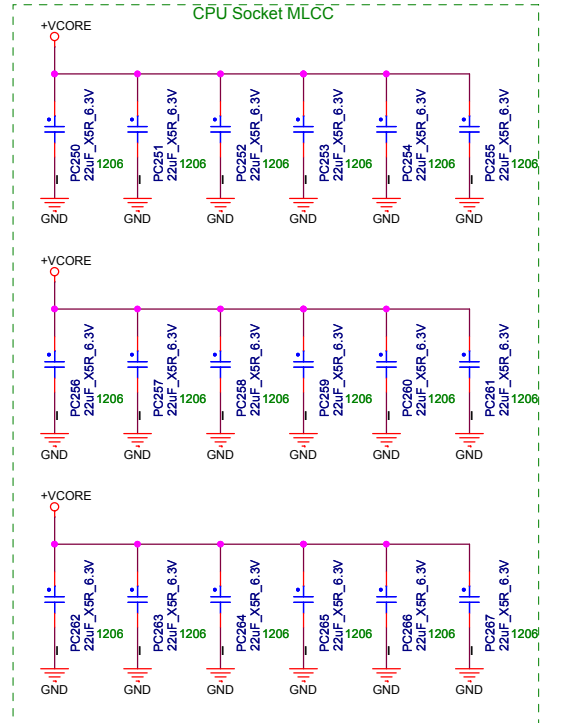
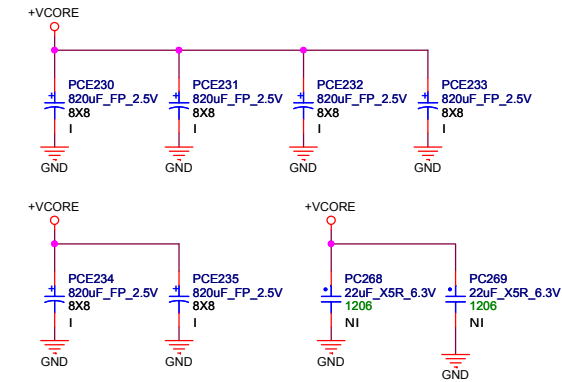
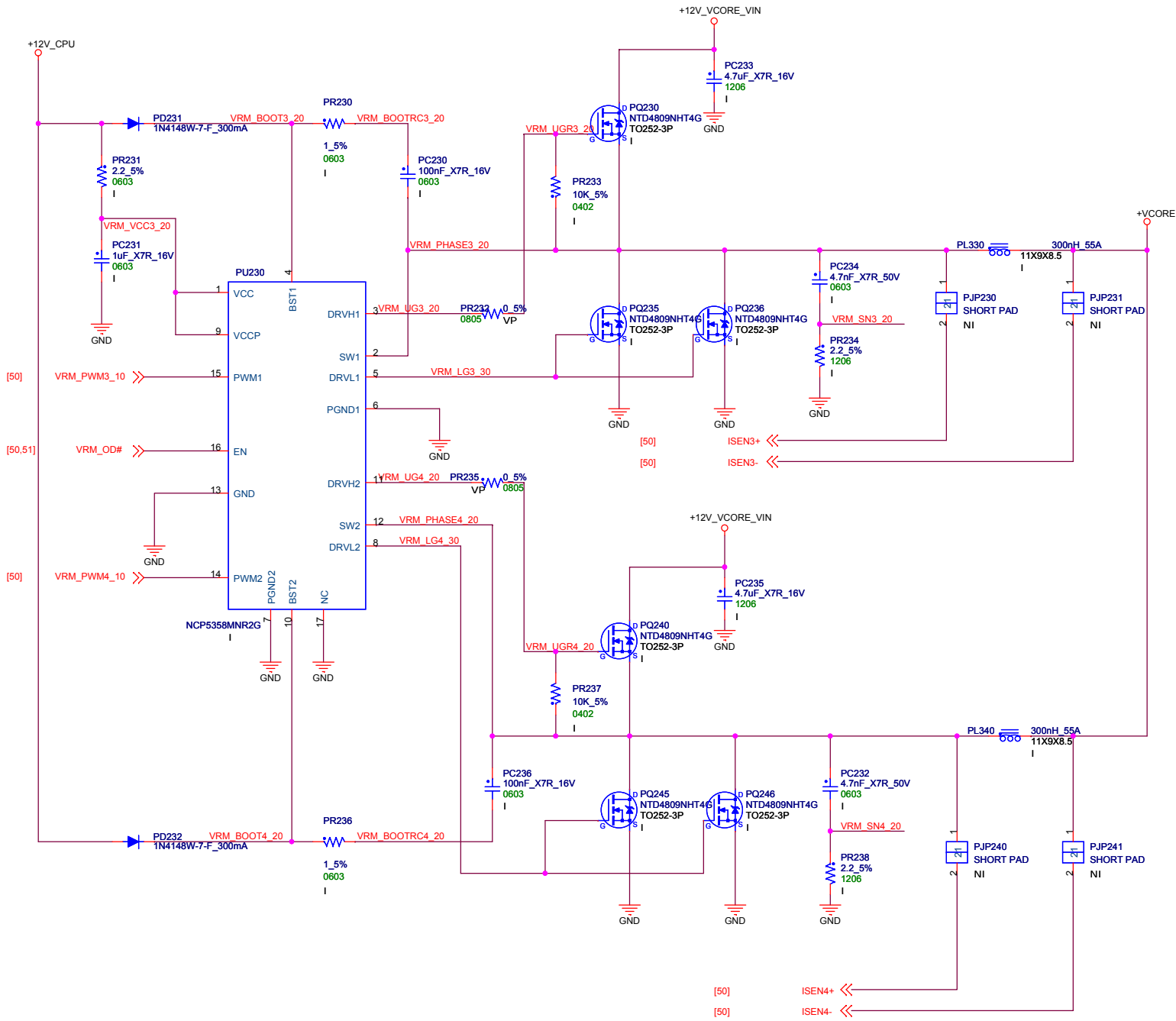
Rev  
**X1**





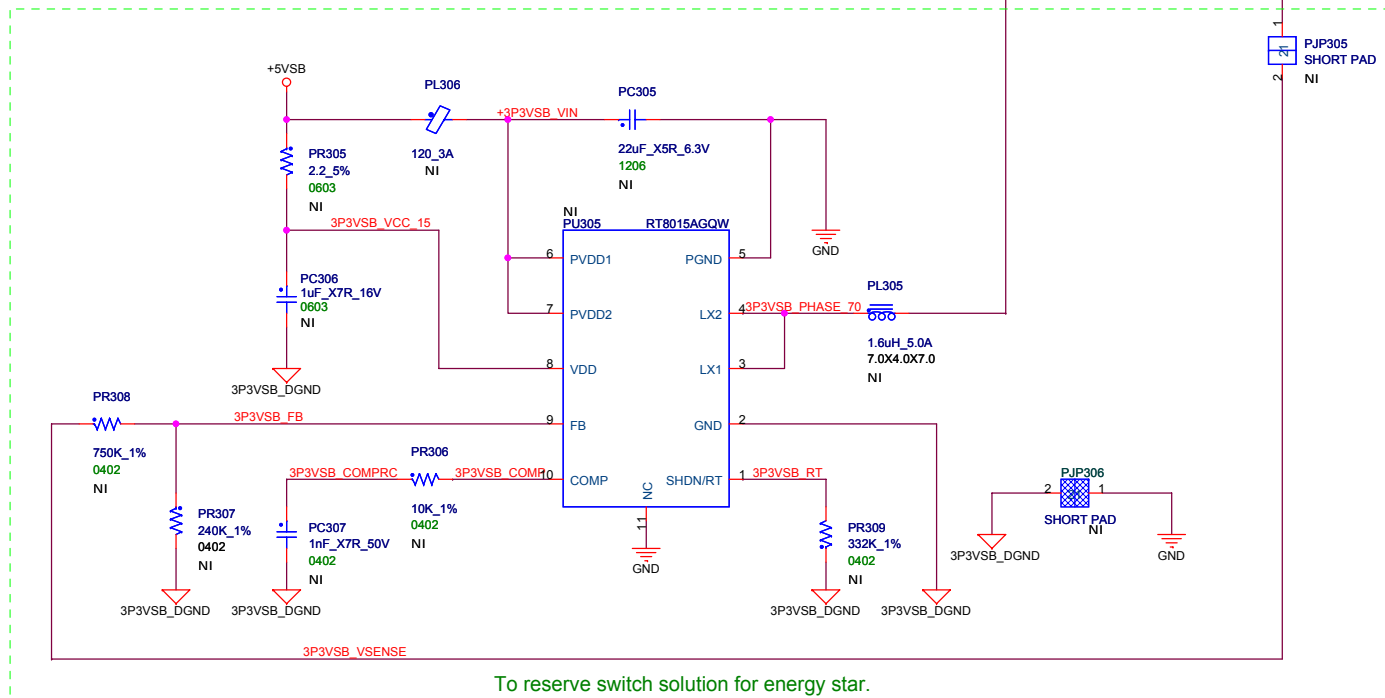
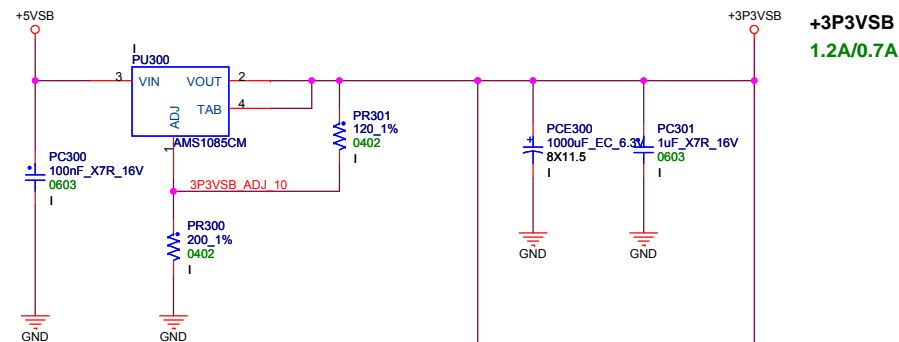


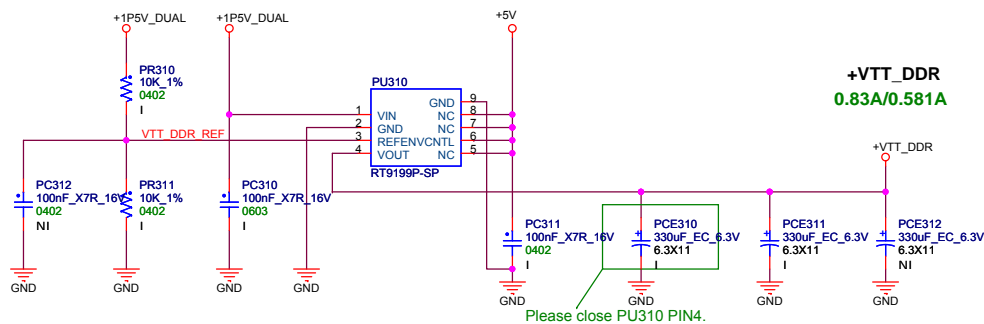
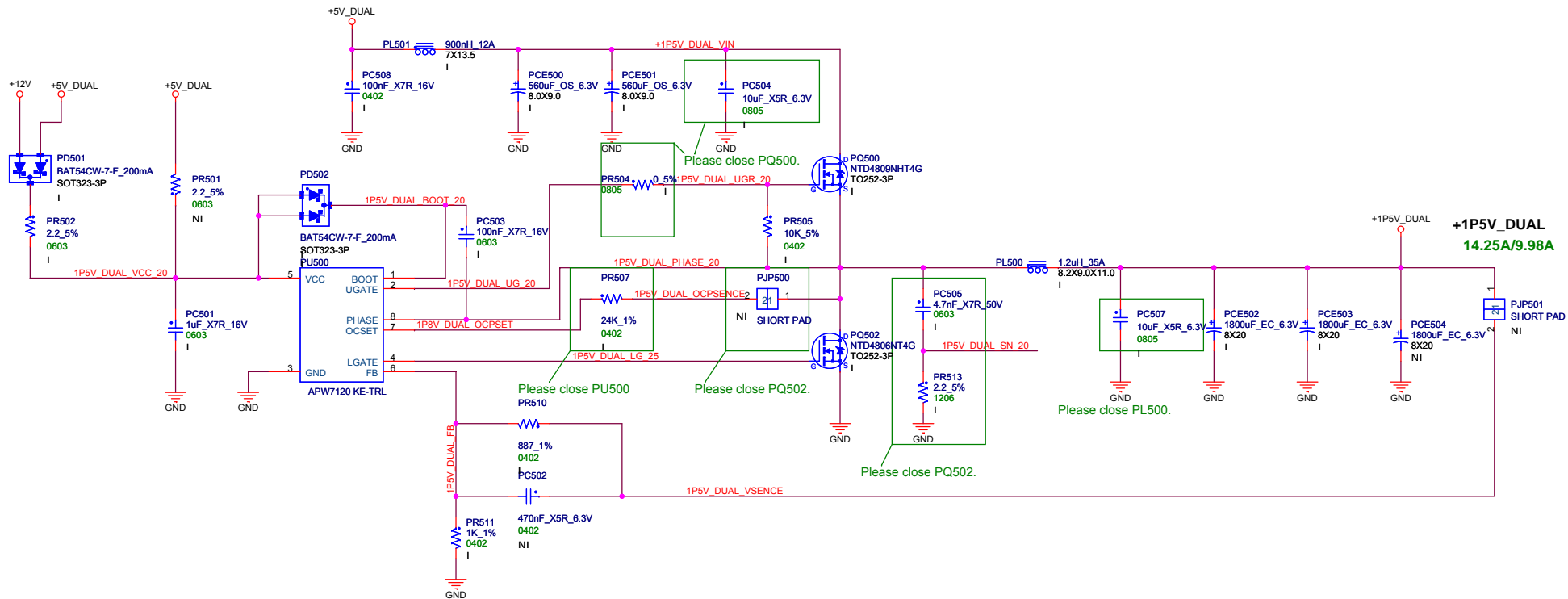






## We need to add 3.3V For MCH VDAC

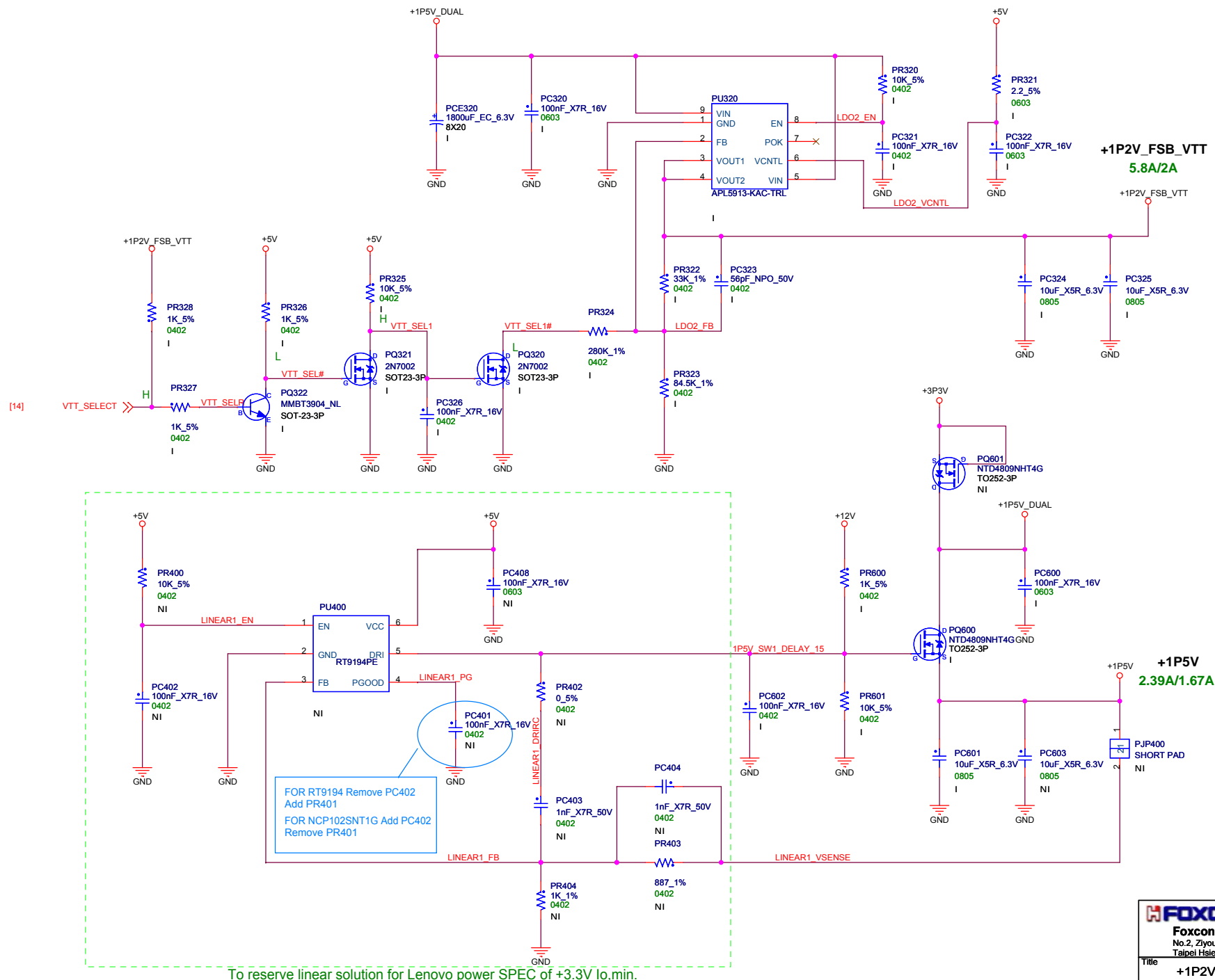




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Title		+1P5V_DUAL & +VTT_DDR	
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Name	Power Plane	Tolerance	Type	Default	Note	Usage
GPI021 SATA0GP	Core	3.3V	I/O	GPI	Pull up 8.2K to 3.3V.	TCM/TPM Header Disable. ( Output )
GPI037 SATA3GP	Core	3.3V	I/O	GPI	Pull up 10K to 3.3V.	TCM/TPM Header GPIO.(I/Out Un-know Waiting Lenovo Feed back)
GPI029 OC5#	Suspend	3.3V	I/O	Native		Waiting Correct USB controller For connection
GPI030 OC6#	Suspend	3.3V	I/O	Native		Waiting Correct USB controller For connection
GPI031 OC6#	Suspend	3.3V	I/O	Native		Waiting Correct USB controller For connection
GPI040 OC1#	Suspend	3.3V	I/O	Native		Waiting Correct USB controller For connection
GPI041 OC2#	Suspend	3.3V	I/O	Native		Waiting Correct USB controller For connection
GPI042 OC2#	Suspend	3.3V	I/O	Native		Waiting Correct USB controller For connection
GPI043 OC4#	Suspend	3.3V	I/O	Native		Waiting Correct USB controller For connection
GPI044 OC2#	Suspend	3.3V	I/O	Native		Waiting Correct USB controller For connection
GPI045 OC9#	Suspend	3.3V	I/O	Native		Waiting Correct USB controller For connection
GPI046 OC10#	Suspend	3.3V	I/O	Native		Waiting Correct USB controller For connection
GPI047 OC11#	Suspend	3.3V	I/O	Native		Waiting Correct USB controller For connection
GPI059 OC0#	Suspend	3.3V	I/O	Native		Waiting Correct USB controller For connection
GPI02 PIRQ#	Core	5V	I/OD	GPI	Pull up 8.2K to 3.3V.	PCI INIT_E#
GPI03 PIRQ#	Core	5V	I/OD	GPI	Pull up 8.2K to 3.3V.	PCI INIT_F#
GPI04 PIRQ#	Core	5V	I/OD	GPI	Pull up 8.2K to 3.3V.	PCI INIT_G#
GPI05 PIRQ#	Core	5V	I/OD	GPI	Pull up 8.2K to 3.3V.	PCI INIT_H#
GPI050 REQ1#	Core	5V	I/O	Native	Pull up 2.7K to 5V.	PCI REQ1# ( For PCI Slot 2 )
GPI052 REQ2#	Core	5V	I/O	Native	Pull up 2.7K to 5V.	PCI REQ2# ( For 1394 )
GPI054 REQ3#	Core	5V	I/O	Native	Pull up 2.7K to 5V.	Non-Usign
GPI051 GNT1#	Core	3.3V	I/O	Native		PCI GNT1# ( For PCI Slot 2 )
GPI053 GNT2#	Core	3.3V	I/O	Native		PCI GNT2# ( For 1394 )
GPI055 GNT3#	Core	3.3V	I/O	Native		CPU_GTLREF_CTRL_1
GPI060 LINKALERT#	Suspend	3.3V	I/O	Native		CPU_GTLREF_CTRL_2
GPI019 SATA1GP	Core	3.3V	I/O	GPI	Pull up 8.2K to 3.3V.	For Lenovo Thermal Sensor ID0
GPI036 SATA2GP	Core	3.3V	I/O	GPI	Pull up 8.2K to 3.3V.	For Lenovo Thermal Sensor ID0
GPI00 BMBUSY#	Core	3.3V	I/O	GPI	Pull up 1K to 3.3V.	PECI_REQ#
GPI09 WOL_EN	Suspend	3.3V	I/O	Native	None. ( Reserve Pull High/Low )	Non-Using
GPI010 CPU_Missing	Suspend	3.3V	I/O	GPI	Pull up 8.2K to 3.3VSB	Non-Using
GPI014 QST_BMBUSY#	Suspend	3.3V	I/O	GPI	Pull up 8.2K to 3.3VSB	LPC_SMI#
GPI015 STP_PCI#	Suspend	3.3V	I/O	Native	None.	STP_PCI# Note3.
GPI026 S4_SATTE#	Suspend	3.3V	I/O	Native	Option to Connect to S4_SLP.	Non-Using
GPI024 MEM_LED	Suspend	3.3V	I/O	GPO	None.	Front Panel LED
GPI058 SPI_CS1	Suspend	3.3V	I/O	GPI	Test Point	Non-Using

Name	Power Plane	Tolerance	Type	Default	Note	Usage
GPI016 DPRSLPVR	Core	3.3V	I/O	GPO	Test Point	Non-Using
GPI023 LDRQ1#	Core	3.3V	I/O	Native	Test Point	Non-Using
GPI049	Core	3.3V	I/O	GPO	Test Point	Non-Using
GPI056	Suspend	3.3V	I/O	GPI	Pull up 8.2K to 3.3VSB	Non-Using
GPI017 TACH0	Core	3.3V	I/O	GPI	Pull up 8.2K to 3.3V	Lenovo SPI write Portect
GPI01 TACH1	Core	3.3V	I/O	GPI	Pull up 8.2K to 3.3V	FRONT_USB_DET#_3
GPI06 TACH2	Core	3.3V	I/O	GPI	Pull up 8.2K to 3.3V	COMM_B_DETECT#
GPI07 TACH3	Core	3.3V	I/O	GPI	Pull up 8.2K to 3.3V	Front Panel LED
GPI08 Unmuxed	Suspend	3.3V	I/O	Native	Pull up 8.2K to 3.3VSB	Non-Using
GPI011 SMBALERT#	Suspend	3.3V	I/O	Native	Pull up 8.2K to 3.3VSB	Non-Using
GPI012 LAN_PHY_PWR_CTRL	Suspend	3.3V	I/O	GPO	None.	Non-Using
GPI013 UnMultiplexed	Suspend	3.3V	I/O	GPI	Pull up 8.2K to 3.3VSB	Super IO PME#
GPI018 UnMultiplexed	Core	3.3V	I/O	GPO	None. ( Reserve Pull High )	Non-Using
GPI035 UnMultiplexed SATACLKREQ#	Core	3.3V	I/O	GPO	Pull up 8.2K to 3.3V None. ( Reserve Pull Down to GND )	Board Rev0
GPI020 UnMultiplexed	Core	3.3V	I/O	GPO	Test Point	Non-Using Note9
GPI038 UnMultiplexed SLOAD	Core	3.3V	I/O	GPI	Pull up 8.2K to 3.3V	TPM_DET#
GPI039 UnMultiplexed SDATAOUT0	Core	3.3V	I/O	GPI	Pull up 8.2K to 3.3V	Lenovo SPI write Portect
GPI022 UnMultiplexed SCLOCK	Core	3.3V	I/O	GPI	Pull up 8.2K to 3.3V	FRONT_USB_DET#_1
GPI048 UnMultiplexed SDATAOUT1	Core	3.3V	I/O	GPI	Pull up 8.2K to 3.3V	FRONT_USB_DET#_2
GPI025 STP_CPU#	Suspend	3.3V	I/O	Native	None.	STP_CPU# Note3
GPI027 UnMultiplexed	Suspend	3.3V	I/O	GPO	Pull up 10K to 3.3VSB	Board ID0
GPI028 UnMultiplexed	Suspend	3.3V	I/O	GPO	Pull down 2.7K to GND	Board ID2
GPI032 UnMultiplexed	Core	3.3V	I/O	GPO	Pull up 1K to 3.3V Pull down 15K to GND	LAN_DISABLE#
GPI033 UnMultiplexed	Core	3.3V	I/O	GPO	Pull up 8.2K to 3.3V	LPT_DET#
GPI034 UnMultiplexed	Core	3.3V	I/O	GPO	Pull up 3.3K to 3.3V	CLEAR CMOS Check CMOS header pull down 4.7K issue

Note9.  
This signal is sampled as a functional strap. See Section 2.25.1 for more details.

Note3.  
Some GPIOs exist in the VccSus3\_3 power plane. Care must be taken to make sure GPIO signals are not driven high into powered-down planes. Also, external devices should not be driving powered down GPIOs high. Some ICH10 GPIOs may be connected to pins on devices that exist in the core well. If these GPIOs are outputs, there is a danger that a loss of core power (PWROK low) or a Power Button Override event will result in the Intel ICH10 driving a pin to a logic 1 to another device that is powered down.

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Title <b>GPIO Function List</b>			
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Clock BIOS Porting Consider:

Drives two device. ( PCI2 )

For Pin4 PCI2 ,pls refer to byte13/bit2 to set=1 to add strength

Drives Three device. ( REF )

1.Byte 9 point out internal bound pad number

2.Byte 13 point out internal I/O pad driver strength.

Therefore, we can understand, if you Byte 9 and Byte 13 to be "1", CV184 will support 3.5X loading.

Device Address  
ASF2.0 Sensor

BIOS Porting Usage


CASE_SENSE_I/O	ICH Intruder ( Option )
	ASF2.0 Sensor ( Default )

Pin Straps  
PCI Express x16 LANE

Enable SDVO and PCI Express

Integrate TPM

Boot Device	SPI
	PCI
	FWH

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